UHD PROJECTOR SYSTEM

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14. ABSTRACT

DTI has devised a display technique that can increase the usable resolution of a microdisplay four to nine times without manufacturing additional pixels. The technique has been shown to produce usable, addressable "virtual-pixels" in excess of the resolution present on the supporting microdisplay.

The Ultra High Definition Projector has four major subsystems: (1) the light engine focuses light into a spot which is made to "jump" between nine positions in a 3×3 array every 1/540th second, forming nine flashing light spots. Light from the spots is directed to a fly's eye lens array. Each lenslet of the fly's eye array forms a microscopic image of the nine spots; (2) The optical system splits light from the flashing spot images in front of each lenslet into three color components, red, green, and blue, and sends each component to one of three Texas Instruments DMD microdisplays. Relay lenses re-image a set of nine flashing spots into each pixel of each DMD. A projection lens projects the image of the spots on the DMD onto a screen; (3)The three Texas Instruments DMDs form images by means of micromechanical mirrors that direct light toward or away from the projection lens; and (4) The interface feeds high resolution images from a computer or camera into a buffer where sub fields are read out in sequence as the light spots flash. The movement of the light spots is synchronized with the operation of the DMD, creating images made up of the light spots.

15. SUBJECT TERMS

Resolution, ultra high resolution, projector, projection, HDTV, quad HDTV, DLP, DMD

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1. INTRODUCTION

This report defines the architecture of the Ultra High Definition (UHD) Projection Display System including functionality, features, and various sub-components of the system. It will summarize the major challenges and accomplishments of the program and make recommendations for the future of the technology and research. This report will address lessons learned and explain any significant departures from the original methodology that was planned. This technical report also details an Interface Design that illustrates how simulations integrate into program documentations and evaluations.

1.1. Definitions, Acronyms and Abbreviations

DVI	Digital Visual Interface
SMPTE	Society of Motion Picture and Television Engineers
DMD	Digital Micro Mirror Display
DLP	Digital Light Projection
LVDS	Low Voltage Differential Signaling
DTI	Dimension Technologies Inc
EDID	Extended Display Identification Data specification
UHD	Ultra High Definition
TI	Texas Instruments
ASE	Applied Science and Engineering
CRT	Cathode Ray Tube
UV	Ultra Violet
RGB	Red, Green, Blue
PDM	Panel Drive Motherboard

2. EXECUTIVE SUMMARY

The Ultra High Definition Projector has four major subsystems:

The ***light engine*** focuses light from a light source into a spot which is made to "jump" from position to position in a 3×3 array every 1/540th second. It includes beam shaping optics used to convert the circular beam to a rectangular beam of the same size and shape as the next component, a double fly's eye lens array. The fly's eye lens has a first array with lenslets of square outline and of the same dimensions as the pixels of a Texas Instruments 1400×1050 resolution Digital Light Processor (DLP). Each lens forms an image of the array of nine flashing spots in front of itself. The second set of lenses, face to face with the first, merely directs light efficiently into a series of relay lenses.

The ***optical system*** serves to re-image each array of nine spots formed by each lens into a pixel of the DLP, and then directs light back out through a projection lens. The optics include a high precision multi-element relay lens system and a series of dichroic prisms that split the light into red, green, and blue components, sending each component to one of three micro displays. A projection lens projects the image on the DLP, made up of the sub-pixel spots, onto a screen.

Three Texas Instruments ***DMDs*** form images by means of micromechanical mirrors that direct light to or away from the optical path to the projection lens.

The fourth component, the ***interface,*** is needed to feed high resolution images from a computer or quad HDTV camera into a buffer where sub fields can be read out in the correct sequence as the light spots flash. Synchronization means are also needed to control the movement of the light spots in conjunction with operation of the DLP and variations in light source intensity used to produce gray scale.

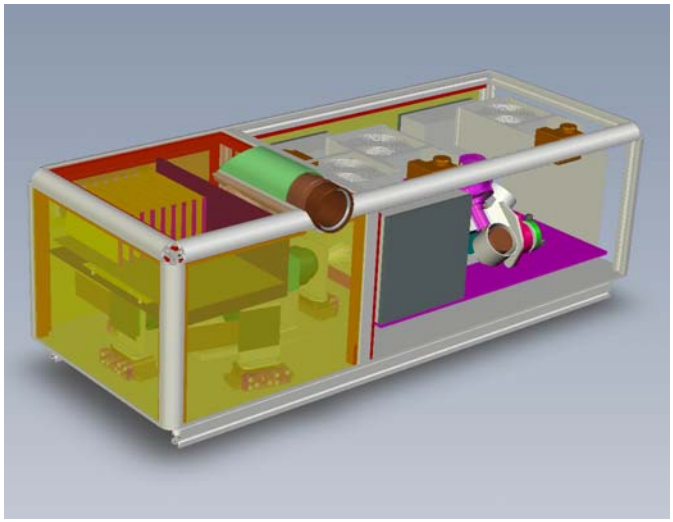


Figure 1 UHD Projector

3. LIGHT ENGINE

At the start of the contract DTI investigated four types of light sources for use in the system. LEDs, arc lamps, conventional lasers, and a new type of VCSEL laser made by Principia Lightworks (the only commercial developers/suppliers of their particular design), were investigated thoroughly throughout the course of the project. Light from arc lamps proved to be difficult to collect efficiently, but one new design made by Wavien proved to be ideal and to have brightness and collection efficiency sufficient for this application. The risk involved with arc lamps was the requirement for some sort of large galvanometric mirror to move the beam being focused by the reflector toward nine different locations every 1/60th second in order to create the nine spots. However previous conversations with Infotonics had indicated that such a galvanometric mirror system was feasible in the sizes and at the speeds required. After weighing the advantages and risks of the arc lamp vs. Principia lasers, it was decided to develop the system using the former.

3.1. LEDs

LEDs were the first light source that DTI investigated. They were quickly rejected due to the fact that the only sources that were bright enough for our purpose emitted light across too large an area and too large an angle for it to be collected efficiently into the light spots required to illuminate the DLP. Following the scope of work DTI moved on to investigating the next possible light source for the project.

3.2. Arc Lamp

DTI's investigations into conventional Arc Lamps led to outsourcing this particular area to an experienced contractor in this field. Oren Sage Technology investigated sources of arc lamps and lamp designs, and held detailed discussions with Wavien, a specialty light engine

manufacturer on the West Coast. Wavien's ray tracing analysis of the required cone angle and size of the fly's eye lenses upon which the light is cast indicated that a 300W Phillips lamp with a 1.3 mm arc could be utilized to advantage over the 200W smaller arc size model. Using this lamp their particular light engine could deliver 12,000 lumens out of the light pipe.

The direction DTI initially pursued was to develop two prototype lamps of Wavien's standard dual parabolic design, consisting of the following components: a dual parabolic reflector, a retro-reflector, a light pipe, a lamp, and the associated mechanical mounting components. The prototypes would have the standard dual parabolic platform with a light pipe and optimized with output apertures to be ascertained by calculations and specifications determined jointly by DTI and Wavien. However, the arc lamp option was abandoned when analysis determined that a necessary component of the system, a large rapidly tilting mirror (described further below) used to make the spot "jump" from position to position, could not be built to specification in terms of speed.

Figure 2 Arc Lamp Without Light Pipe

3.3. Conventional Laser

Several vendors of conventional lasers used in projectors were contacted, but such lasers proved to be too bulky and too expensive in the power ranges that would be required for the scope of work for the system. There were no options for conventional lasers meeting the brightness requirements that could be obtained.

3.4. Custom design eVCSEL Laser

DTI investigated a new type of laser called an eVCSEL laser which was being developed by Principia Lightworks. The Principia lasers had unique advantages in the form of lack of speckle and an electron beam pumping system whereby the electron beam could be deflected across a flat laser crystal like an electron beam in a CRT to form various illumination patterns, such as the sequentially flashing spots required for the present application. Principia's eVCSEL lasers thus remained an attractive, potentially low cost option, but represented a risk in that they were not commercially available products and only red lasers had been demonstrated in fully functional form. Green and blue had, however, been demonstrated in the lab and Principia's development schedule indicated that they would be available well within the timeframe required to construct DTI's system. DTI therefore contracted with Principia to supply two red lasers as soon as possible, and then two green, and two blue lasers as they became available, plus all control electronics necessary to deflect the electron beam and create the nine lasing spots, plus power supplies.

The proposed Principia laser system consisted of seven major components, all of which except the fully functional green and blue lasers had been demonstrated and are described below.

As Principia's effort progressed, it became apparent that Principia was unable to supply all the required equipment in a timely fashion. In order to proceed forward with the project without more delays it was evident that DTI take on some of the development work under a non-disclosure and non-compete agreement with Principia, including the design and construction of a compact Faraday cage, design of an electronics board, and heavy assistance in designing other boards. DTI also devised a gray scale generation pattern that could produce 256 gray levels per color in such a way that used light efficiently, and investigated and implemented scanning patterns to write the spots in as small a size as possible on the laser crystals without overheating the crystals. These investigations and components are described below.

3.5. eVCSEL Lasers

Principia Lightworks had developed and patented a laser technology, the eVCSEL: an electron-beam-pumped Vertical Cavity Surface Emitting Laser, which can serve as a platform light source for display and industrial applications. The eVCSEL laser can be fabricated at any desired wavelength from the UV through the visible. The eVCSEL takes the form of a laser faceplate that is attached to a standard cathode ray tube ("CRT"). This combination allows for high power output, low power consumption, and significantly lower cost manufacturing than competitive laser technologies. Furthermore, scanning eliminates laser speckle given that the pixels are not mutually coherent. A unique feature of this laser is the ability to scan the electron beam across the faceplate in the same manner that an electron beam is scanned across the surface of a CRT, allowing a laser light emitting image to be formed in a manner similar to the way an image is formed on a CRT. DTI used the electron scanning feature to move the electron beam in circular patterns to create each of the nine light spots in sequence.

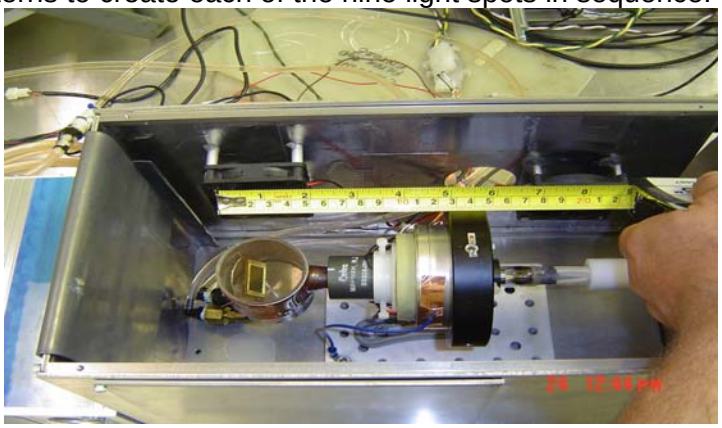


Figure 3 eVCSEL Laser

3.6. Faraday Cage

The Faraday cage controls the three laser tubes, one red, one green and one blue. It provides a -35KV potential for the cathode of each laser tube as well as grid voltages to regulate electron gun emissions.

The major components of the Faraday cage include: Faraday cage chassis and insulation barrier, Chopper board and isolation transformer, Faraday cage controller, Pulser board/G1 combo, G2/G3 combo, and Heater regulator

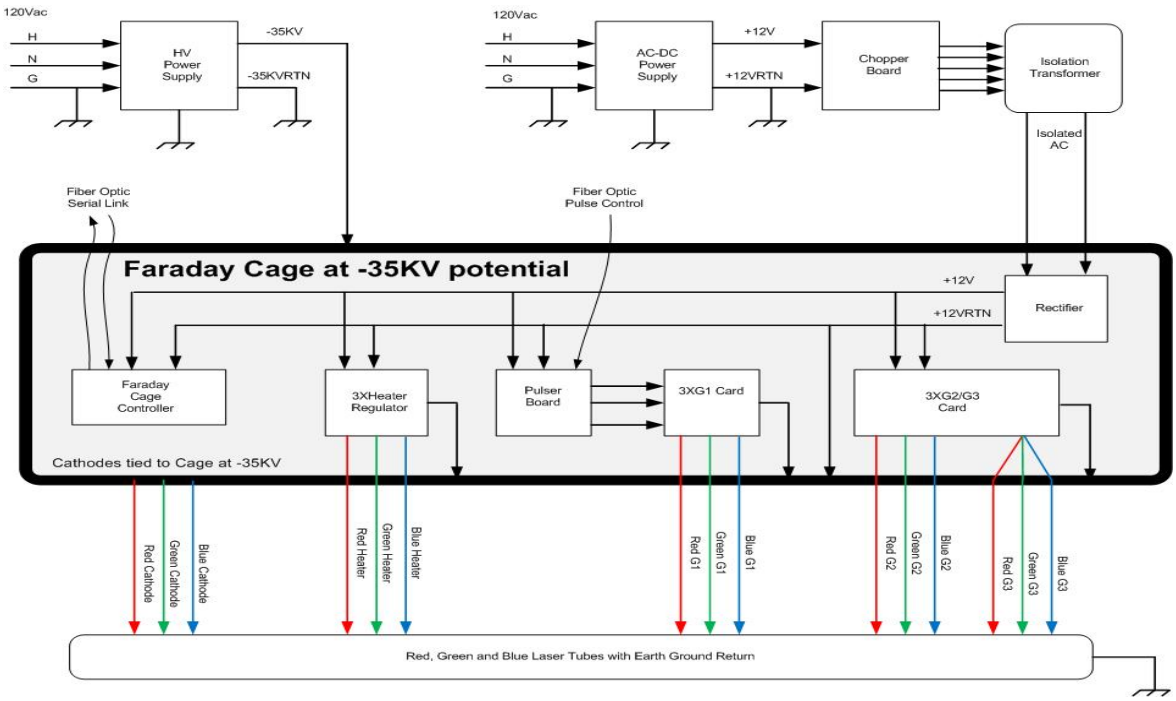


Figure 4 Faraday Cage Block Diagram

3.6.1. Faraday Cage Chassis and Insulation Barrier

The chassis of the Faraday cage is biased at -35KV relative to earth ground by an external high voltage power supply. The Faraday cage is insulated from any -35KV return path by an epoxy box that surrounds the Faraday cage. Any gaps, mating surfaces or holes in the Faraday cage or insulating barrier are protected from arcing by ensuring any potential arc path length is > 1.5". All of the -35KV electrical connections to the inside of the Faraday cage are made at one common location.

3.6.2. Chopper Board and Isolation Transformer

The Faraday cage and any electronics inside have -35KV potential relative to earth ground. To power electronics inside the Faraday cage an isolation transformer provides a floating low voltage AC source with isolation from the -35KV. The chopper board creates the isolated low voltage AC signal by pulsing DC from an external DC power supply into the primary side of the isolation transformer. The AC output from the secondary side of the isolation transformer is brought to the inside of the Faraday cage and is rectified and the resulting negative side of the DC output is tied to the Faraday cage chassis, providing a +12Vdc source for powering the low voltage electronics inside the Faraday cage.

3.6.3. Faraday Cage Controller

The Faraday cage controller controls and monitors the operation of the electronics inside the Faraday cage via a full duplex fiber optic serial link. The functions of the Faraday cage controller include: Monitor internal Faraday cage DC voltage, Monitor internal Faraday cage temperature, Set/monitor individual red, green and blue G1 voltages, Set/monitor individual red, green and blue G2 voltages, Set/monitor common RGB G3 voltage, Set/monitor individual red, green and blue G1 bias voltages, and Set/monitor individual red, green and blue G1 pulse top voltages

3.6.4. Pulser Board/G1 Combo

The pulser board monitors a fiber optic input signal to regulate the G1 drive control for each laser. The fiber optic signal transports a synchronized pulse train that is used by the pulser board to generate a weighted amplitude over time signal to drive the G1 voltage. The fiber optic link transports G1 pulse edge timing and pulse width, and the sync signal to synchronize the repeating G1 drive level pattern. This is used by the G1 card to vary the level of each laser output for generation of gray scale images. Additionally, a periodic "heartbeat" must be present in the fiber optic signal or the pulser board will not enable the G1 drive voltage.

The Optical signal transported over the fiber optic cable should always be at one of 3 levels:

- Level 1: Full ON – 100% of full on, nominal fiber optic transmitter/receiver pair normal operating level
- Level 2: 1/2 ON – 50% of full on
- Level 3: Baseline – 0% of full on, no light transmitted

The pulser board monitors the incoming optical levels and derives gray scale pattern synchronization and pulse width. The duration of each level must be present within certain min/max limits before the G1 drive output will be enabled by the pulser board. The rising edge of all full scale and ½ scale pulses are monitored and integrated to set the rising edges of the pulses in the G1 drive signal. The full-scale level pulse defines the start of the repetitive encoded gray scale pattern. The pulse width of all full scale and ½ scale pulses are monitored and integrated to set the pulse width of the G1 drive signal. The repetitive input pattern of one full scale pattern followed by eleven ½ scale pulses is also used as a "heartbeat" to ensure the laser does not drive unless the deflection system is operating properly. The pulser board disables the G1 drive if the heartbeat is not detected.

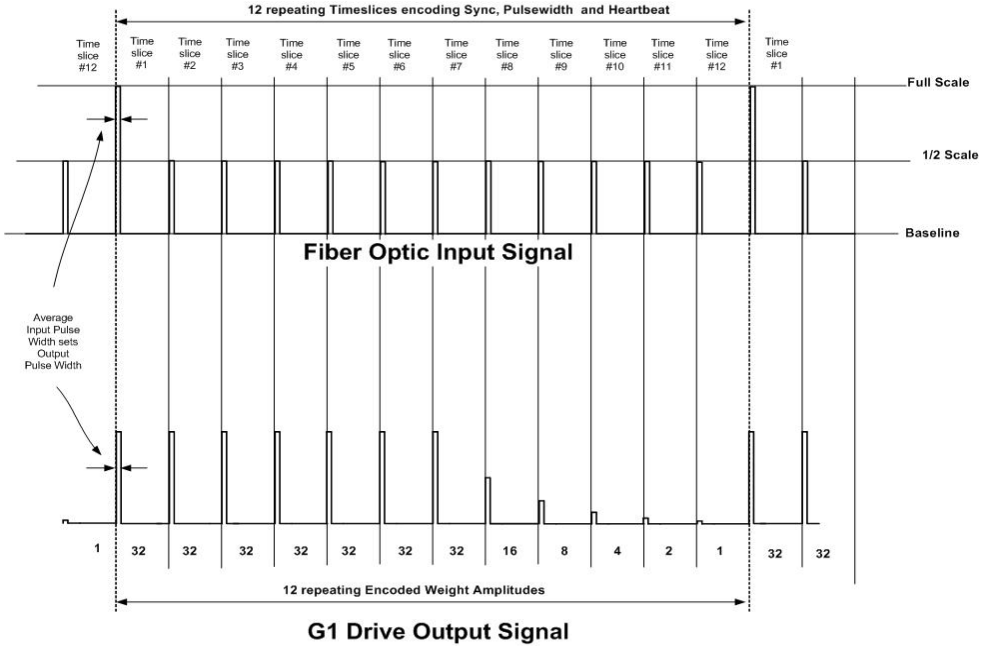


Figure 5 Fiber Optic Transport of Gray Scale Generator Sync

If the pulser board detects the heartbeat, and the amplitude and pulse width of the incoming fiber optic signal meets the constraints of the expected repetitive pattern then it drives the G1 board with an encoded amplitude G1 drive pattern providing a weighted amplitude over time. By turning mirrors in the DMD display to either "reflect light" or "don't reflect light" position during

any of the 12 time slices of the weighted G1 drive pattern generation of a synchronized gray scale level from 0-255 can be created. The following example shows how a gray scale level value of 31 (out of 0-255) is created by the DMD to the "reflect light" position during time slice periods #8-12 while turning them to the "don't reflect light" position during time slice periods #1-7.

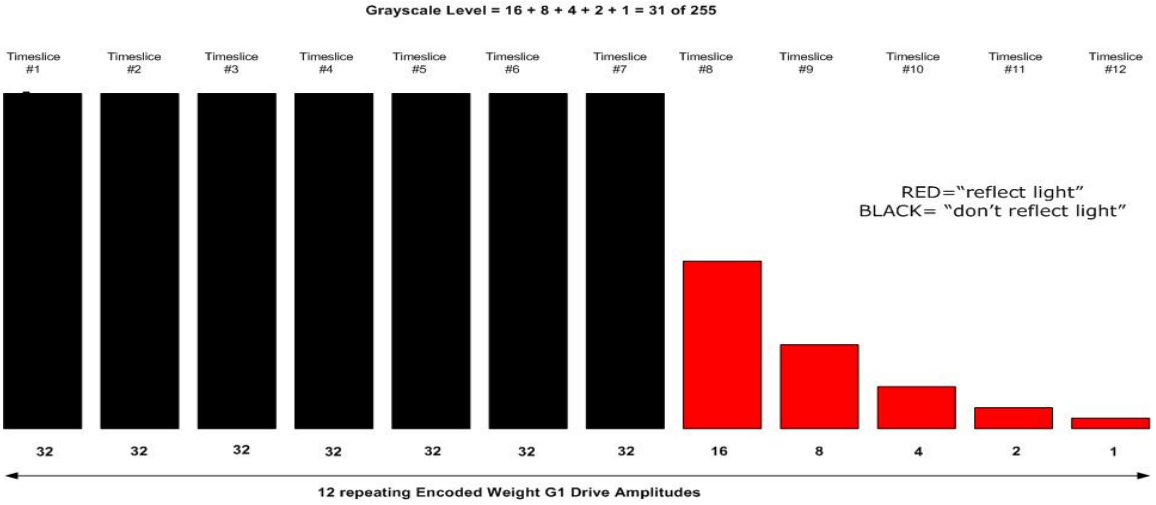


Figure 6 Example of Encoded Gray Scale Level 31 of 255

Any gray scale level from 0-255 can be created by turning the mirrors in the DMD to either the "reflect light" or "don't reflect light" position during the appropriate 12 time slices of the weighted amplitude G1 drive pattern. The G1 board has a high speed video amplifier that can drive the grid 1 input on the laser tube with a high slew rate analog voltage from -200v to 0v. The signal source for the video amplifier is the weighted amplitude pattern output from the pulser board. The G1 board has adjustments for setting the cutoff voltage for each laser and the gain of the video amplifier. These adjustments will allow a fixed pattern output from the pulser board to be tailored to the unique characteristics of each laser tube. The adjustments will be controlled via the Faraday cage controller.

The Faraday cage controller controls adjustments for setting the output voltage of the G1 power supply, cutoff offset and video amplifier gain. The G1 power supply has a low voltage monitor point that the Faraday cage controller uses to monitor the HV power supply output.

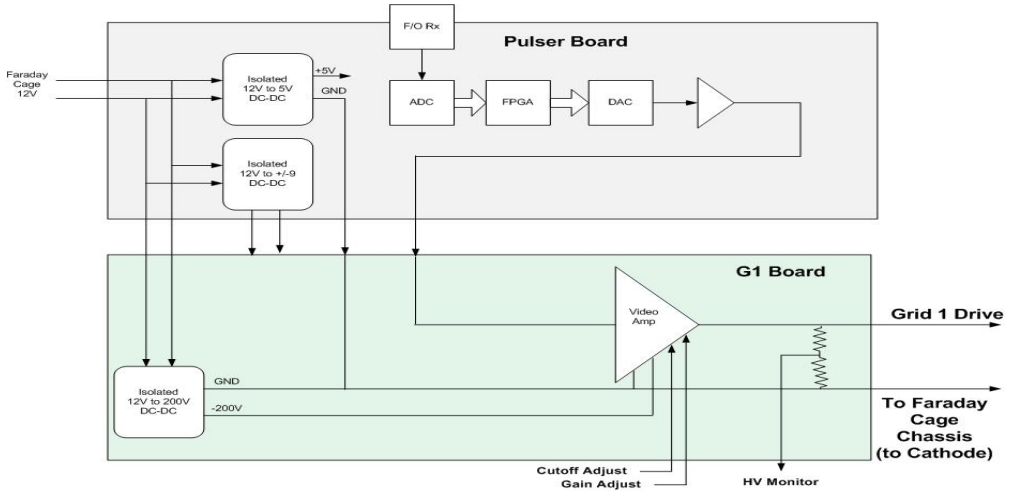


Figure 7 Pulser Card/G1 Card Combo

3.6.5. 3XG2 /G3 Combo

The 3XG2/G3 combo board provides three individual G2 voltages and one common G3 voltage for grid 2 and grid 3. The Faraday cage controller controls adjustments for setting the output voltage of the four HV power supplies. Each of the four output voltages has a low voltage monitor point that the Faraday cage controller uses to monitor the HV power supply outputs.

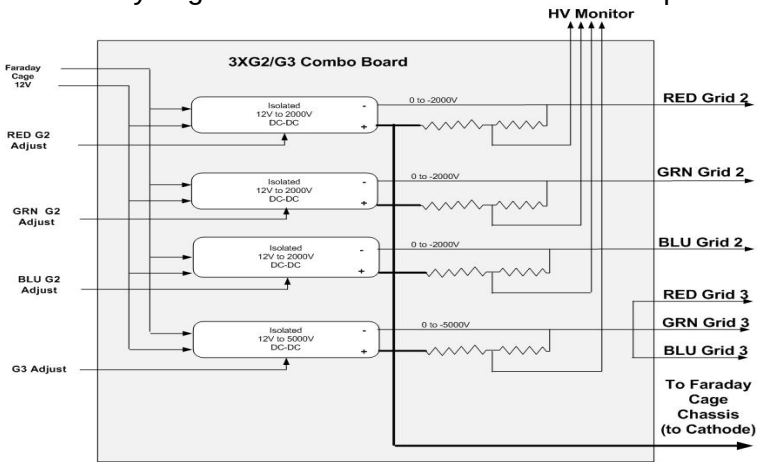


Figure 8 3XG2/G3 Combo Card

3.6.6. Fiber Optic Monitor Board

The fiber optic monitor board independently monitors the fiber optic drive signals and turns the G1 voltage to 0 volts within 1 microsecond if the heartbeat pulses are not detected.

3.6.7. 3X Heater Regulator Board Fiber

The 3X heater regulator board provides three independent filament heater constant current sources.

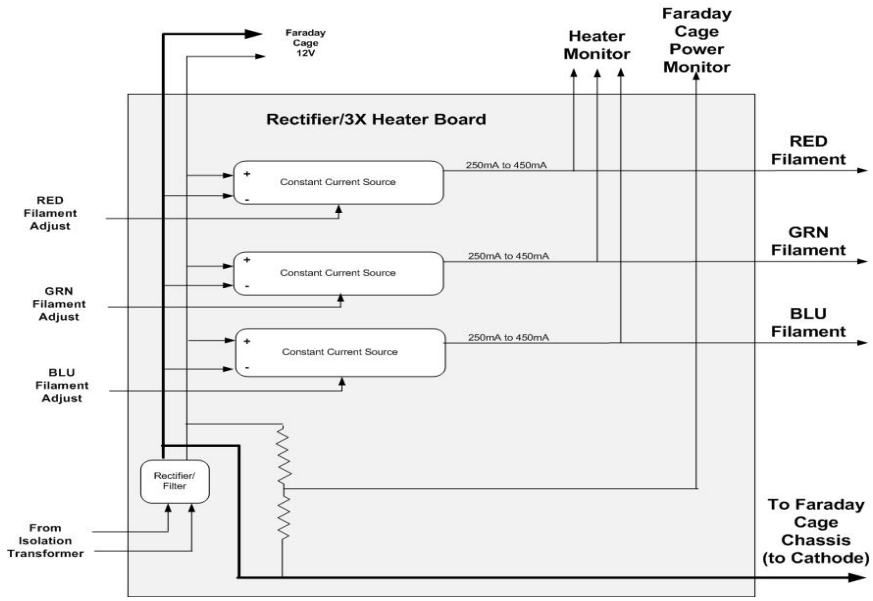


Figure 9 3X Filament Heater Current Source

3.7. Thermal Management Monitors

The **thermal management** functional block prevents the deflection system drive electronics and the laser crystals from overheating. Strategically placed temperature sensors are electronically monitored to ensure the temperature does not exceed a pre-determined threshold for that sensor. If a detected temperature exceeds its threshold an alarm is declared and the ability to operate the UHD projection display system will be suspended until the temperature at the sensor is lowered below a lower threshold. The thermal management functional block also includes multiple ac fans that will circulate forced air through the chassis to dissipate heat that is generated by the system power supplies and electronics.

Two independent circulating liquid cooling systems are provided for maintaining safe operating temperatures of the deflection drive system amplifiers and the laser tubes.

3.7.1. Liquid Cooling System

The deflection system **liquid cooling** system provides heat dissipation for the six deflection amplfiers with heat exchangers plumbed in series. The temperature of the circulated liquid for each cooling system is monitored by the system Controller by reading a temperature sensor in-line with each return line.

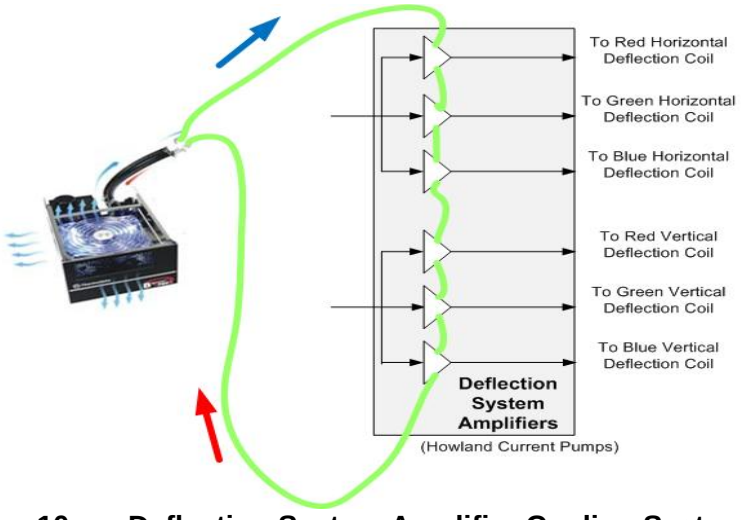


Figure 10 Deflection System Amplifier Cooling System

The laser tube liquid cooling system provides heat dissipation for the red, green and blue laser tubes which are plumbed in parallel. The temperature of the cooling systems can be monitored by the system controller by reading a temperature sensor in-line with the return line.

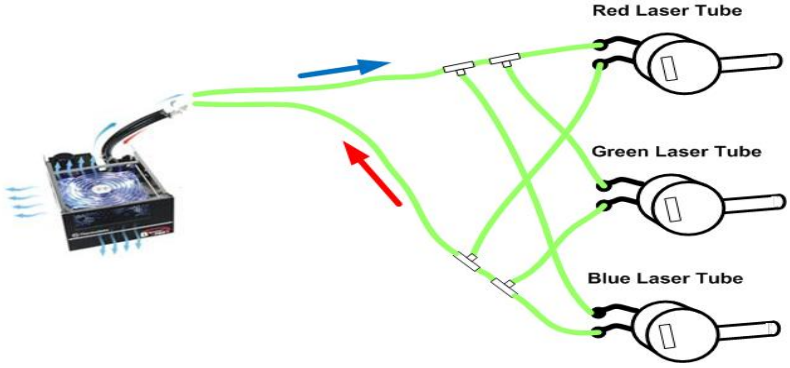


Figure 11 Laser Tube Cooling System

3.7.2. Forced Air Cooling System

A forced air cooling system is provided for maintaining safe operating of electronics within the UHD cabinet. A thermal sensor on the panel drive motherboard can detect the ambient temperature of the electronics inside the UHD projector cabinet.

3.7.3. System Hazards

Generating high intensity light capable of creating high resolution projection images requires the use of red, green and blue lasers excited by electron guns. High voltage and potentially harmful levels of laser light require special safety systems. A safety interlock system is required to ensure all safety protection features are functional. A system controller and monitoring circuitry ensures that the RGB laser outputs power are within safe operating range. The UHD system will only generate laser light when the safety monitors are satisfied and safety covers are present.

3.8. Light Engine Troubleshooting

When the red lasers were delivered and the related power supply built and tested, the lasers did not lase. Initial problems were traced to the high voltage power supply. It became apparent that the power supply and electron tube used to pump the laser were far from a turnkey system. After much effort including two visits by the vendor's CEO/chief scientist and electronics engineer, it was still impossible to get the lasers to lase properly, except for brief intervals in the case of one of the red lasers. The lasers did glow dimly, allowing verification of the operation of the scanning system and its ability to write spots in sequence onto the laser crystals, plus initial alignment of the optical system. After several months of trying and replacement of several burned out lasers, DTI was forced to abandon the Principia lasers as an illumination source.

Due to lack of additional funding having been granted a second contract extension, DTI was forced to change the Statement of Work and move forward with a single channel monochrome projector system. Investigation revealed that a single monochrome conventional laser could be obtained within the remaining budget. These lasers did not have the brightness required for a real projector, but would have enough brightness to demonstrate the system. This meant that DTI had to revisit the design of Optics I and investigate beam deflection systems suitable for use with a laser. After determining that a redesign was feasible and a suitable galvanometric laser deflection system could be obtained, DTI chose and ordered a green laser made by Shanghai Dream Laser. An anti-speckle system was also necessary for use with this type of laser. An anti-speckle system consisting of a diffuser rotated rapidly by an electric motor was demonstrated on the optical bench.

4. OPTICAL SYSTEM

4.1. Optics I – A (Beam shaping and spot movement)

Oren Sage Technology at first devised a first order design concept for beam shaping optics for use with the Wavien arc lamp (from circular lamp beam to rectangular image designed to match the size and shape of the double fly's eye lens) based on the use of a light pipe beam homogenizer, combined with a rapidly tilting mirror designed to cause the spot from the lamp to move rapidly between nine positions, plus optics that would focus all light into a rectangular double fly's eye lens (see below). The design was optimized by placing the mirror on axis, which allowed the mirror to be as small as possible. The first order design is shown in the drawing below.

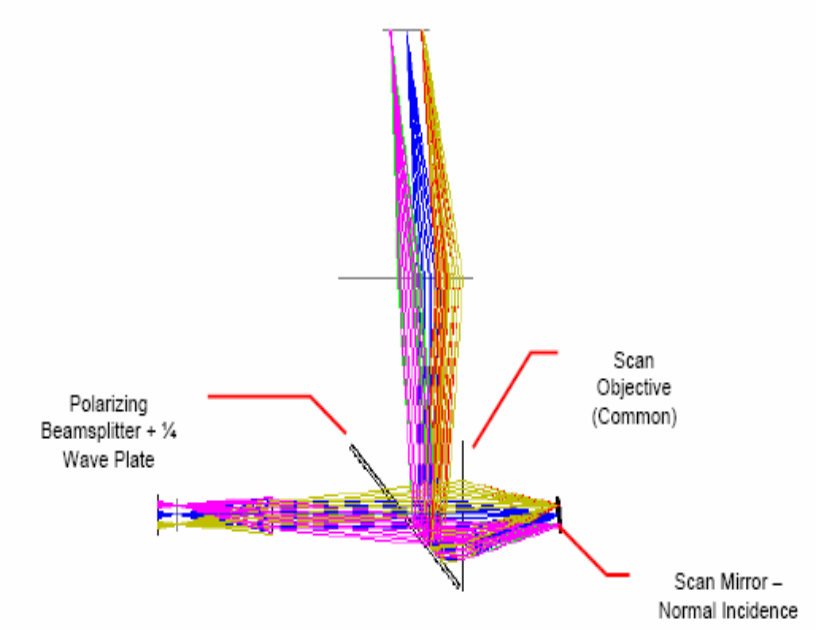


Figure 12 Beam Shaping Ray Trace

Light comes from the light source on the left. If required, a field lens (the first lens shown) in front of the light source aims the light at the entrance pupil of a condenser lens. The light source is the field stop for the system. The condenser lens collimates the light. It provides the aperture stop for the system. Light next passes through a polarizing beam splitter and becomes P polarized, and through a ¼ wave plate which causes it to become RH circularly polarized. The scan objective forms an image of the light source at the flipping mirror and as light exits back through it; it also forms a real image of the aperture stop beyond the scan mirror at the spot plane. The scan objective also takes light from the scan mirror and re-collimates it. Note that after passing through the wave plate a second time, the light is now S polarized and therefore is reflected from the beam splitter. The last lens forms an image of the flipping mirror (and therefore the light source) at the fly's eye lens plane, and it also makes the light from the spot plane appear to come from infinity. As the scan mirror tilts, the image of the aperture stop (the spot) moves around the spot plane which causes the light impinging on the fly's eye lens assembly to come in from different angles.

4.1.1. Gray Scale Shutters

The gray scale system used with the DLP must rely on a light source that varies in brightness between at least 8 levels. Since an arc lamp is incapable of such rapid brightness variations, an LCD shutter system was investigated for this purpose. Based on preliminary quotations and discussions with shutter manufacturers and consideration relative to the operation of the DLP, a preliminary design for the shutter was devised. The shutter would be mounted on the lamp side of the fly's eye lens assembly, and possess sixteen independently controlled strip shaped sections parallel to the long side of the lens array. These sixteen independently controlled sections were to be activated one after the other as the DLP was scanned, essentially following the scan down the display and providing the maximum amount of time during each scan when any given part of the shutter is open, instead of having to wait for all the pixels on the DLP to be scanned and change state before going through its on/off cycle.

4.1.2. Flipping Mirror

Various designs for the flipping mirror were investigated by Infotonics. They all involved a thin, flat, ~25 mm diameter light weight aluminized mirror mounted on a double gimbaled system, allowing tilt across several degrees in both the X and Y directions.

After consideration of several designs and analysis of two design iterations it was determined by Infotonics that the system would not be capable of the rapid flipping rates that were initially calculated and which were necessary for the system. Infotonics proposed investigating other options but without any guarantee that these would work either. The arc lamp illumination design was therefore abandoned in favor of the backup option in the form of the Principia lasers.

4.1.3. Piezo Stage System

An alternative spot movement system was briefly investigated with the assistance of vendors. This consisted of a piezoelectric stage that moved the double fly's eye lens, and thus the spots formed by it, rapidly between nine positions. Analysis indicated that this type of system would not be fast enough.

4.2. Optics I – B (Redesign)

When the arc lamp illumination design was abandoned in favor of the backup option in the form of the Principia lasers, the illumination device was changed from the Wavien lamp to the Principia lasers. This change resulted in a beam shaping system redesign to accommodate the new illumination devices. The new layout is illustrated in the ray trace in Figure 13 and operates as follows:

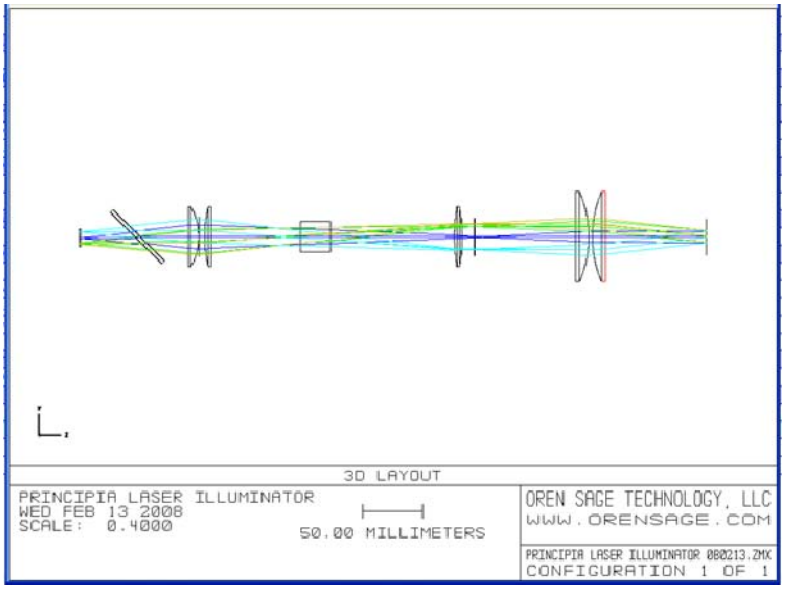


Figure 13 3D Optical Layout using Principia Laser Illuminator

Light from the nine spots formed by each laser (one laser is shown on the left) is directed by a double Plano convex lens through a color combining cube, which combines the red, green, and blue light from the lasers into white light. Aperture stops are also located at the cube faces. The Plano convex lenses, in combination with a third double convex lens, also focus the light spots at a plane in front of another set of larger Plano convex lenses (on the right) which collimate the light from the spots and direct it onto the fly's eye lens, shown at the far right of the ray trace.

4.3. Optics I – C (Redesign)

Ultimately the Principia laser system failed and had to be replaced by a single color conventional laser. This was within specification of the change in SOW and the Optics I system had to be redesigned again. Fortunately, this redesign was more of a component elimination process. The beam shaping task was simpler with the conventional laser system. The back end of the beam shaping assembly used for the Principia system was removed and replaced by the laser, a simple miniature galvanometric mirror device, and a spinning de-speckle diffuser behind the fly's eye lens array. Components in front of the fly's eye lens (between it and the Optics II relay lens system) were retained without modification

4.3.1. Beam Shaping Mirror System

Two mirrors were used to allow the laser to be placed to one side within the existing enclosure, and to direct its beam to a galvanometer. After striking the galvanometer, the beam was deflected to nine spots in sequence through the existing double convex lens, where it was focused onto a spinning 10 degree FWHM diffuser that acted as a de-speckling device. Light exiting the diffuser continued on to the collimating lens and fly's eye lens as previously designed.

4.3.2. Galvanometer

An off-the-shelf galvanometer was chosen to drive an X-axis and Y-axis servo mechanism in the laser beam (which was ultimately intended to be the combined beam of 3 lasers, red, green, and blue) to direct the laser beams to nine different spot locations in sequence. The servo mechanism is a two axis galvanometer with a small 5 mm mirror that directs the laser beam to a position based in low voltage X-axis and Y-axis input signals. Due to the small size of its mirror and related mountings, this galvanometer could easily meet the speed requirements for mirror movement.

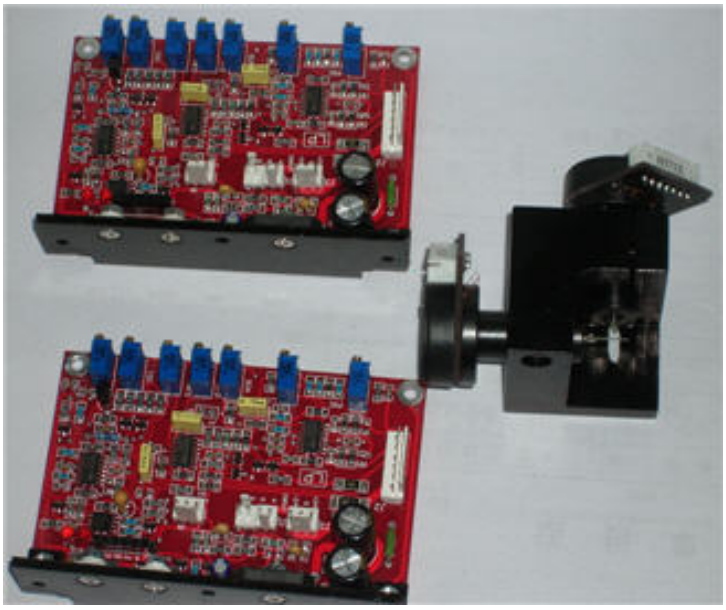


Figure 14 Galvanometer Interface

The galvanometer interface consists of two waveform generators that generate repetitive control signals that are synchronized to the rest of the UHD System through differential clock and sync input signals from the panel drive motherboard.

The laser beam is periodically moved to one of nine different locations to create the light spots which are re-imaged by the double fly's eye lens into "sub-pixels" on each mirror of the DMD. A horizontal step waveform generator that is synchronized to the system sync signal creates three different levels for moving the laser beams to one of three columns. This signal drives the horizontal galvanometer. A vertical step waveform generator, also synchronized to the system sync, signal creates three different levels for moving the laser beams to one of three rows. This signal drives the vertical galvanometer.

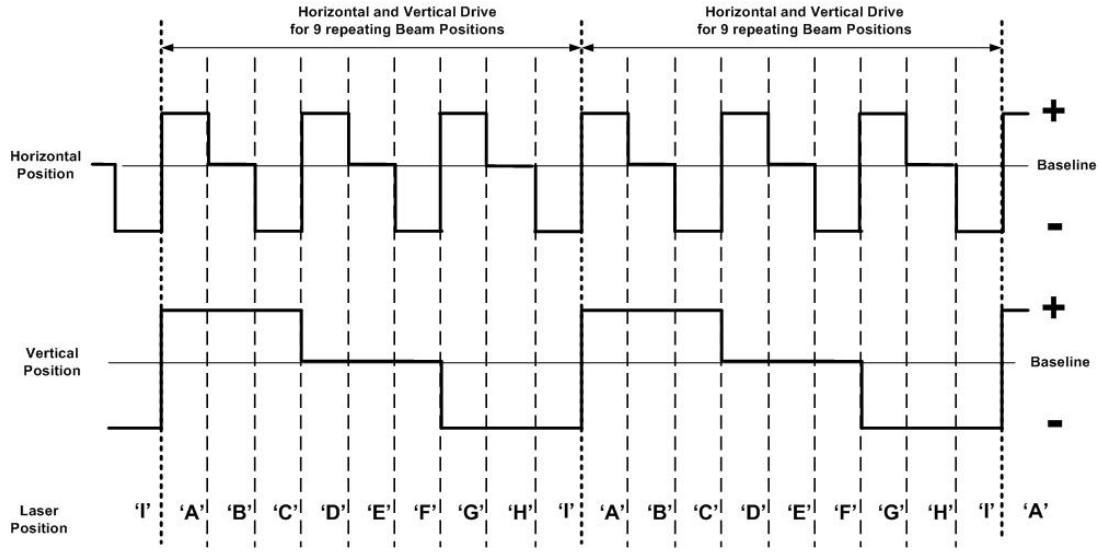


Figure 15 Horizontal and Vertical Galvanometer Drive

The nine different positions are used to create nine sub-pixels for each of the 1.47 million mirrors in the Discovery 3000 DMD. The laser beam stays in each location long enough for the gray scale generator to cycle through twelve time slices that allow 256 gray scale levels to be encoded. The time in between positions is kept to a minimum to allow the maximum time for sub-pixel illumination.

4.4. Optics II

The Optics II system was designed to re-image the multiple spot images formed by the fly's eye lens onto the pixels of the three DLPs. It required precise lenses in order to focus light into spots of at most 5 microns diameter into precise position on the 13.68 micron wide pixels of the three DLPs. Light also had to be directed through a color beam splitting prism assembly without the introduction of astigmatism, and means to accommodate the DLP's off-axis imaging requirements had to be devised.

DTI contracted ASE Optics to design and build the relay optics to image the spots created by the fly's eye lens onto the DLPs. ASE had quoted the work prior to DTI obtaining the contract, but the decision to use Texas Instruments DLPs complicated the design. Due to the need to either send light onto the DLP at an off-axis angle or intercept it going out at an off-axis angle. All off-axis systems investigated proved to be very bulky and very complex. ASE finally devised a solution in the form of a beam deflector – basically a Fresnel prism placed immediately in front of the DLP, which would deflect light entering and exiting the DLP and would allow use of conventional on-axis relay lenses. Since the system was initially going to rely on a broad

wavelength halogen lamp, certain aspects of the lens system had to be very complex in order to focus all wavelengths in three color bands accurately. Later, the switch to laser illumination allowed some parts to be simplified, but much design time had been spent in accommodating the more difficult initial halogen illumination system. Fabrication by ASE's vendors also took longer than expected. Toward the end of the program, one vendor proved to be incapable of fabricating one component, the beam deflector, to spec. The problem was traced to the replication process used to create the plastic part from a mold. A second vendor with a more precise replication process was contacted, but their charge for precision replication was beyond the remaining budget of the program.

The Optics II system remained virtually unchanged through the various incarnations of the illumination system and Optics I, except for a simplification of the beam deflectors allowed by the switch to narrow bandwidth lasers.

4.4.1. Double Microlens Array

The double microlens array is used to image light from the light source into over one million moving spots of light, which are in turn re-imaged onto the pixels of the DLPs by the relay lenses. Each microlens array consists of an array of 13.68 um square outline lenses arranged in straight rows and columns across a 30 mm × 25 mm substrate. For ease of fabrication, the lens coverage was extended all the way to the edges of the glass. As a bonus this would allow the same microlens to be used with future, HDTV resolution DLPs. The two microlenses were mounted lens side to lens side, with their lenses one focal length apart (41 um). The purpose of this arrangement was to cause the light exiting the array to be focused into a tight square shaped far field pattern which can be focused into the relay optics.

4.4.2. Relay Lenses

The relay lenses are used to refocus the red, green and blue components of the image of the spot array formed by the fly's eye lens onto the pixels of the red, green, and blue channel DLPs. They also serve to re-image the DLPs, illuminated by the light spots, onto the focal plane of the projection lens. There are five multi element relay lenses, as shown. All five are identical. Together, they form a symmetrical optical system that sends light through each of three color channels. Light travels through two of these lenses on the way to each of the DLPs and through two lenses on the way back out to the projection lens.

Figure 16 Relay Lens System

4.4.3. Polarizing Prism

A polarizing prism is used to reflect light coming back through the red, green, and blue channel relay lenses upward through the last relay lens and on through the projection lens.

4.4.4. Correcting Plate

The correcting plate is used to correct the astigmatism introduced by the beam deflector.

4.4.5. Polarization Retarder

The polarization retarder is used to turn the light polarization by 90 degrees after it passes through the retarder twice (once on the way to the DLPs, then once on the way back) so that on the way out it will be reflected by the polarizing prism into the projection lens, instead of going back to the fly's eye lens.

4.4.6. Dichroic Prism

The Dichroic Prisms are used to send the red, green, and blue light through three separate relay lenses to the three DLPs. Each of the DLPs creates one of the color components (red, green, or blue). The prism also recombines the light reflected from the three DLPs on the way out, so that the three color DLPs are superimposed on each other at the focal plane of the projection lens, forming a single color image.

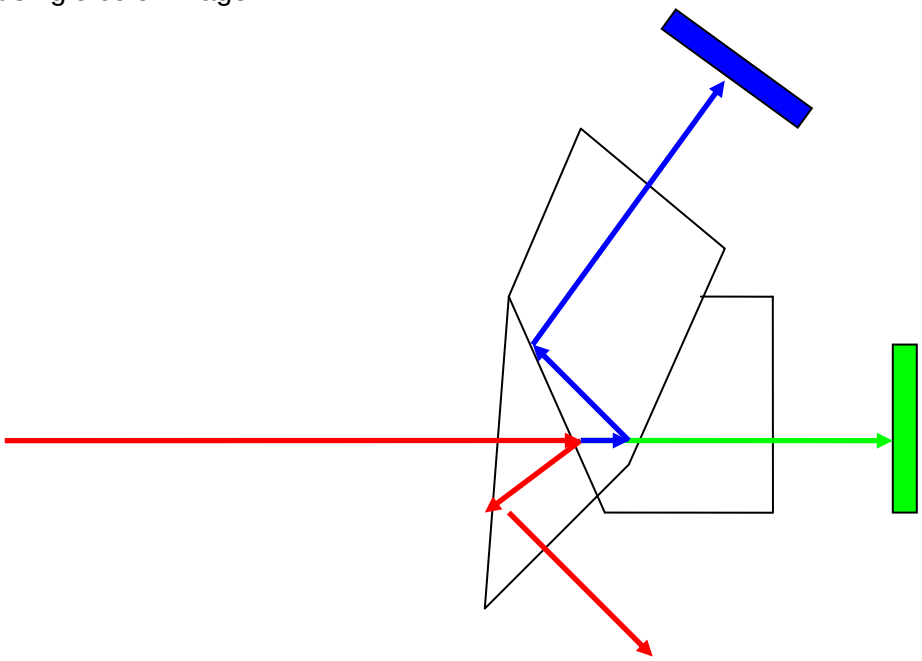


Figure 17 Dichroic Prism

4.4.7. Beam Deflector

A unique beam deflector, basically a Fresnel prism, was designed to be placed immediately in front of each DLP. The function of this deflector was to change the angle of the light entering the DLP to 18 degrees off normal, since the DLPs are designed to accept light from 18 degrees off axis. Mirrors in the "on" (in this case tilted) condition reflect light back at 18 degrees off axis where it was deflected back to the normal direction and out through the relay lenses by the beam deflector.

4.4.8. Projection lens

DTI initially purchased a precision f/4 projection lens at the recommendation of ASE Optics. However, it was ultimately decided that a larger image with a shorter throw distance would be required for demonstrations. Therefore a second off-the-shelf projection lens was obtained. This second lens was a 50 – 70 mm, f/2.5 mm zoom lens which produced a larger image for a given throw distance.

5. DIGITAL MICRO MIRROR DISPLAY

5.1. Discovery 3000 Virtex – 4 FPGA Function

The Discovery 3000 Virtex-4 FPGA interfaces to the DMD Interface through the Discovery 3000 expansion connectors via the panel drive motherboard. In the UHD system, three individual TI Discovery 3000 DLP adapters drive individual red, green and blue digital micro mirror displays (DMD). The Discovery 3000 Virtex-4 FPGA provides system timing and synchronization to the DMD interfaces, DVI receiver Interfaces and the deflection system. The video information from the DMD Interface is transferred to the Discovery 3000 Virtex-4 FPGA over 64 LVCMOS signals at 100 MHz

5.1.1. FPGA Timing

5.1.1.1. FPGA Timing Generator

The DVI data transfer from the DMD interface to the Discovery 3000 FPGA is synchronized by using a VHDL module that is common to the Discovery 3000 FPGA, the DMD interface FPGA, and the laser interface FPGA. The VHDL module “cnts.vhd” is clocked by the incoming 50MHz SYS_CLK signal and synchronized by the 30 Hz SYS_SYNC signal. Counters are generated by this module that allows decoding of timing required for synchronization to the incoming 64 bit video data bus.

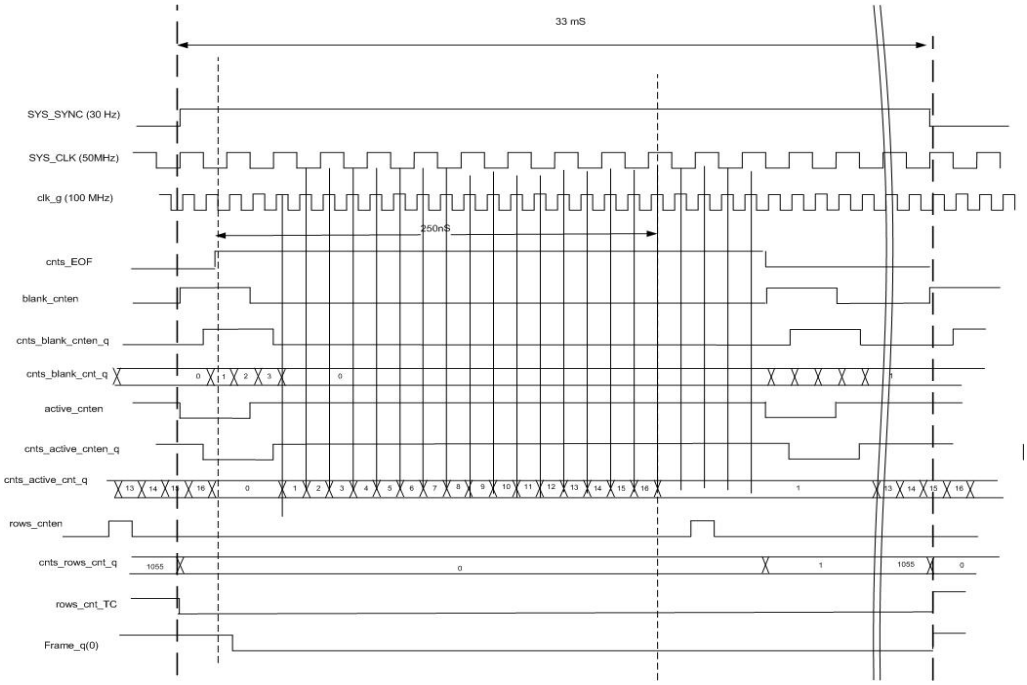


Figure 18 SYS_CLK and SYS_SYNC Inputs and Timing Generator Outputs

5.1.1.2. Discovery 3000 FPGA Pattern Generator

For testing, the Discovery 3000 Virtex-4 FPGA can generate patterns on the DMD, independent from the DMD Interface 64 bit interface. Twelve control bits driven by the DMD interface and connected to the Discovery 3000 FPGA through the panel drive motherboard are used for selecting modes and patterns.

5.1.1.3. Discovery 3000 Video Data Sequencing

The Discovery 3000 FPGA does not buffer the data received from the DMD interface module. The images have been "pre-buffered" by the DVI and DMD interfaces to sequence directly into the DMD and create gray scale and increased resolution.

5.1.2. FPGA Discovery 3000 Virtex-4 FPGA Design

One 668 pin Virtex-4 FPGA on each Discovery 3000 controls the DVI data to DMD conversion of one color for the UHD projector. Each Virtex-4 FPGA is dedicated to receiving input from its associated DMD Interface module and to driving one DMD. Three Discovery 3000 modules are used in the system.

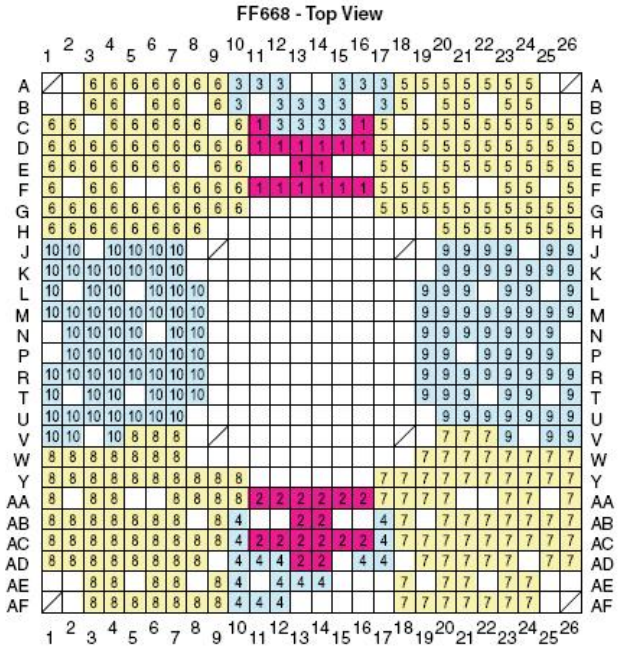


Figure 19 Virtex-4 XC4VLX25-668 I/O Banks

5.1.2.1. Discovery 3000 FPGA I/O Bank Partitioning

The Discovery 3000 application FPGA transfers red, green, or blue DVI data to the DMD for each RGB color. The FPGA I/O banks are partitioned to provide various types of electrical interfaces for different interface functions:

Bank 5, 6, 7, 8 expansion connector, Bank 9 – SYS_CLK, SYS_SYNC
Bank 0, 7, and 8- DMD connector, Bank 1 – Test points and LEDs

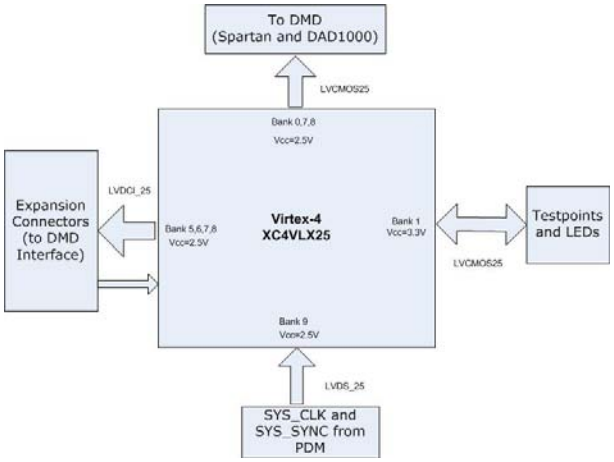


Figure 20 Discovery 3000 FPGA I/O Banks

- **FPGA I/O Bank 5, 6, 7, 8 – DMD Interface Board**

Banks 4, 5 and 6 of the Discovery 3000 Virtex-4 FPGA are configured as 2.5V single ended and differential I/O and are dedicated to transferring the images from the DMD interface board to the DMD for that color.

- **FPGA I/O Bank 0, 7, 8 – DMD Drive**

Bank 0, 7, and 8 is configured as 2.5V Differential I/O and drives the Spartan FPGA and DAD 1000 devices that control the DMD display.

- **FPGA I/O Bank 1 – Test points and LEDs**

Bank 1 is configured as 2.5V and used for general purpose use for testing.

- **FPGA I/O Bank 9 – DYD_CLK and SYS_SYNC inputs**

Bank 9 is configured as 2.5V differential I/O and receives the system clock and sync signals from the panel drive motherboard.

6. INTERFACE DEVELOPMENT

6.1. Panel Drive Interface

The Panel Drive Motherboard (**PDM**) is a “motherboard” PCB that interfaces nine DVI Rx interface PCBs with one laser interface, three DMD interface PCBs and three TI Discovery 3000 DLP adapters for driving individual red, green and blue Digital Micro Mirror Displays (DMD). The panel drive motherboard provides system timing and synchronization for the DVI Interfaces, DMD interfaces, Discovery 3000s, and the laser interface. An OEM USB interface allows system control and status monitoring of the modules in the system.

6.1.1. PDM FPGA Overview

A 256 pin Altera Cyclone II EPF2C5F256C6 FPGA provides System Timing for the UHD Projection System. It generates and distributes clock, sync and control data to the laser interface, DVI interfaces and DMD interfaces. The FPGA I/O is partitioned to provide various types of electrical Interfaces for different Interfaces.

Bank 0 – DVI Interface CNTL_DIN, Bank 1 – Test points/LEDs, Bank 2 – USB Interface Connector, Bank 3 - DMD Interface Connector, Bank 4 – DVI Interface Connector

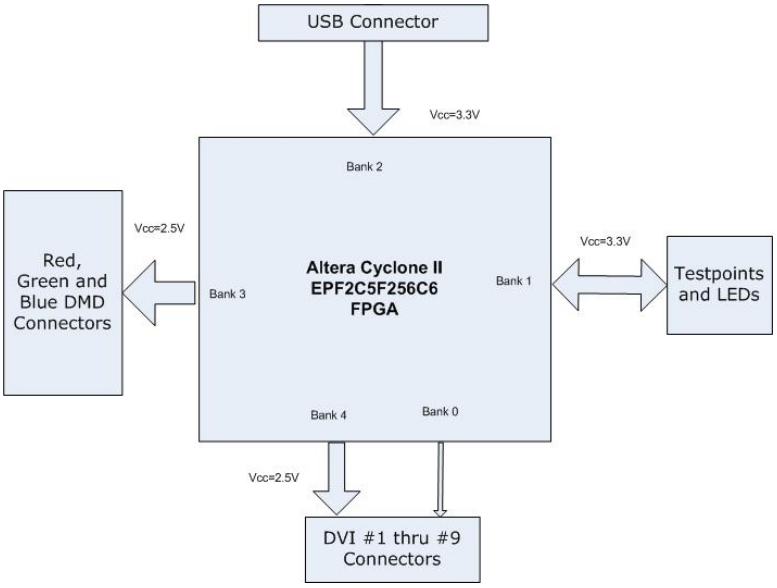


Figure 21 Panel Drive FPGA I/O Banks

FPGA I/O Bank 0 – DVI Interface CNTL DIN Interface
Bank 0 of the Panel Drive Motherboard DMD FPGA is configured as 2.5V single ended and is dedicated to the Serial Control Interface DIN function.

FPGA I/O Bank 1 – Misc. /Test point Interface
Bank 1 of the Panel Drive Motherboard DMD FPGA is configured as 2.5V single ended and is dedicated to LED Indicators, miscellaneous use and as logic analyzer and oscilloscope test points.

FPGA I/O Bank 2 – USB/GPIO Interface
Bank 0 is configured as 3.3V CMOS I/O and is connected to a Hirose FX8-80S-SV connector that can be used to Interface to a QUICKUSB module for general control and status monitoring of the FPGA during development, or general purpose I/O for control and monitoring of system operation.

FPGA I/O Bank 3 – Differential Clock/Sync/CNTL DIN Interface
Bank 3 is configured as 2.5V Differential I/O and transports the SYS_CLK, SYS_SYNC and CNTL_DIN to the red, green, and blue DMD interfaces. Bank 3 also transports the SYS_CLK, SYS_SYNC and CNTL_DIN to the Laser interfaces.

FPGA I/O Bank 4 – Differential Clock/Sync Interface #1 thru #9
Bank 4 is configured as 2.5V Differential I/O and transports the SYS_CLK and SYS_SYNC to DVI Rx Interfaces #1 thru #9

6.1.2. DVI Interface connections to DMD Interface

The 8 bit red, green and blue video data from all nine DVI RX interface PCBs is distributed to the three DMD Interface PCBs on the PDM via 16 bit differential pairs. One DMD interface PCB processes the incoming data and manages an image buffer that transfers the data to a 3000 DLP adapter dedicated for the RED component of the Video. Identical DMD interface PCBs and image buffers transfer the data to two additional Discovery 3000 DLP adapters dedicated for the GREEN and BLUE components of the video. Each DVI Rx interface PCB

encodes the 8 bit data on the incoming DVI input as 12 bit gray scale time slice values. These values are stored in 12 different sections of the image buffer, with each section containing a gray scale weight of the complete 1400 × 1050 sub-pixel image for that color. When these 12 gray scale weighted images are written to each Discovery 3000 DLP adapter in a sequence that is synchronized with a repeating laser intensity pattern, a gray scale level from 0-255 can be created for the original 8 bit DVI image for each color.

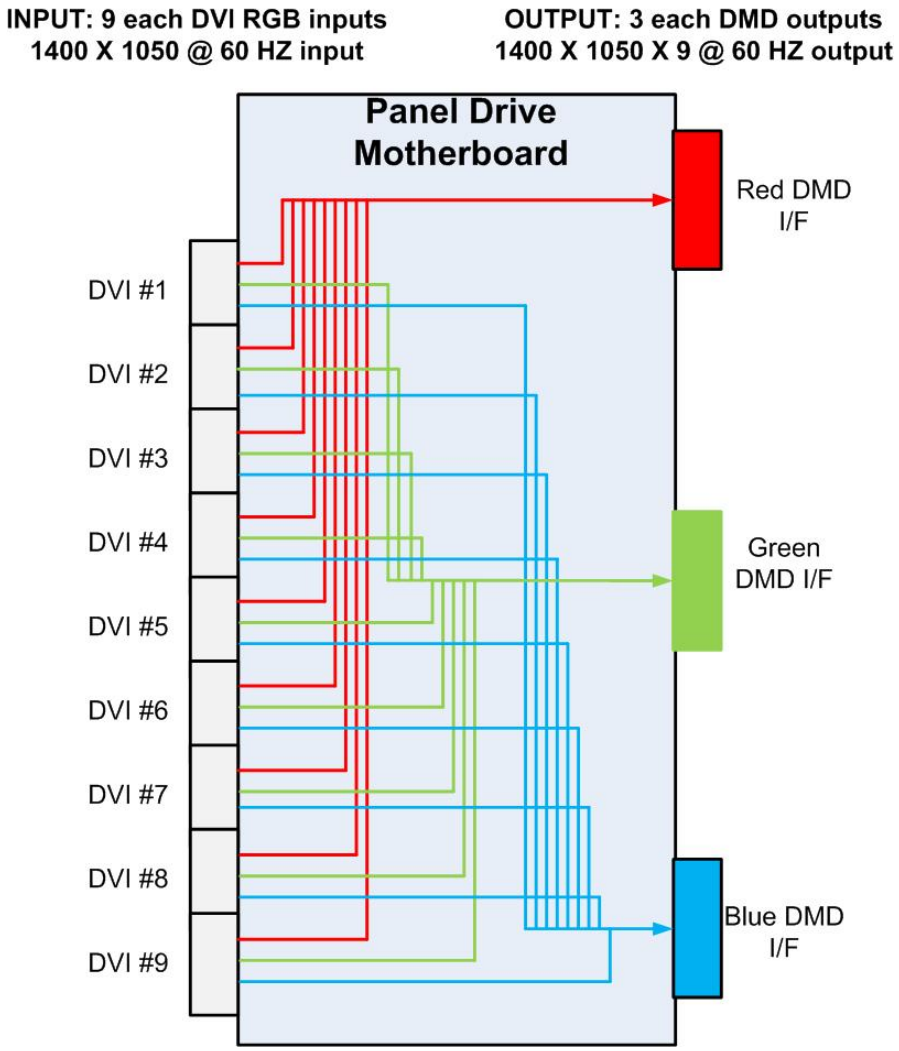


Figure 22 PDM Distribution of DVI input RGB to DMDs

6.1.3. SYS_CLK and SYS_SYNC Generation/Distribution

A single FPGA on the PDM controls the timing and control of the other boards in the UHD System. A 50 MHz oscillator on the PDM provides a reference for all system timing and SYS_CLK is distributed to other modules in the System. The FPGA creates a SYS_SYNC signal that is distributed to other modules in the System to ensure all data transfers between modules are synchronized. The VHDL module “i_cnt.vhd” is common to the PDM FPGA, the laser interface, the DVI interface and the DMD interface FPGAs to ensure synchronization of timing throughout the system.

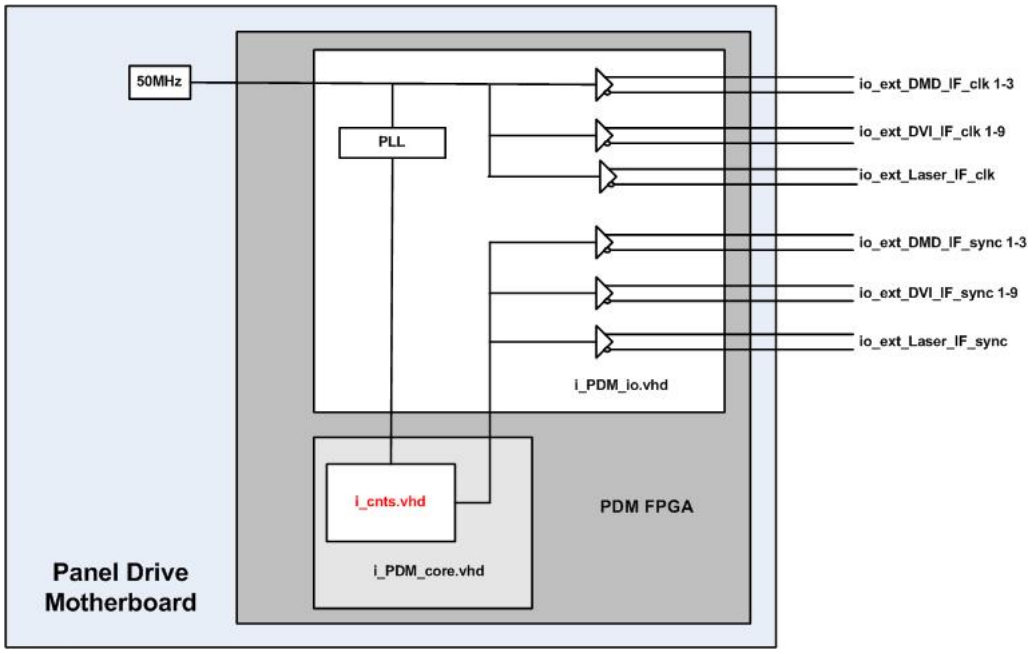


Figure 23 PDM SYS_CLK and SYS_SYNC Distribution

6.1.4. System Control/Monitor USB Interface

A high speed OEM USB input/output interface module is connected to the panel drive motherboard to allow control and monitoring of the UHD system and its components.

- The Bitwise QuickUSB Module (QUSB) board provides a simple, "plug-in", solution for connecting hardware to a P.C. The board provides 20 bits of user-configurable digital I/O, a 90Kbps I^2C Interface, and an 8 bit wide data bus for fast FIFO transfers.

The target Interface consists of:

- One 8 or 16-bit high-speed parallel port (HSPP)
- Up to five general-purpose 8-bit parallel I/O ports
- Two RS-232 compatible ports
- One I2C master port
- One soft SPI master port supporting up to 10 slave devices
- One FPGA configuration port (Altera PS or Xilinx SS)

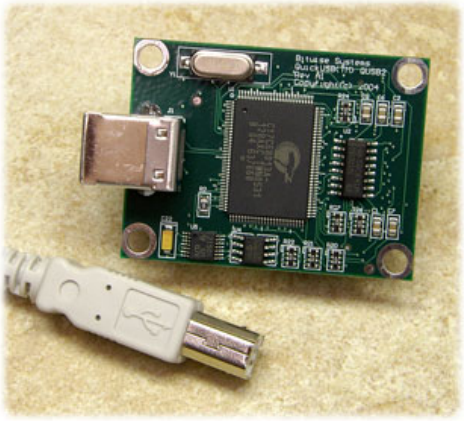


Figure 24 QUSB I/O module

The QUSB I/O module interfaces to the PDM FPGA to create a group of memory mapped 16 bit registers that can be written to by the PC. The FPGA transfers these registers to independent serial control interfaces for the laser interface PCB, each of the nine DVI interface PCBs and the three DMD interface PCBs.

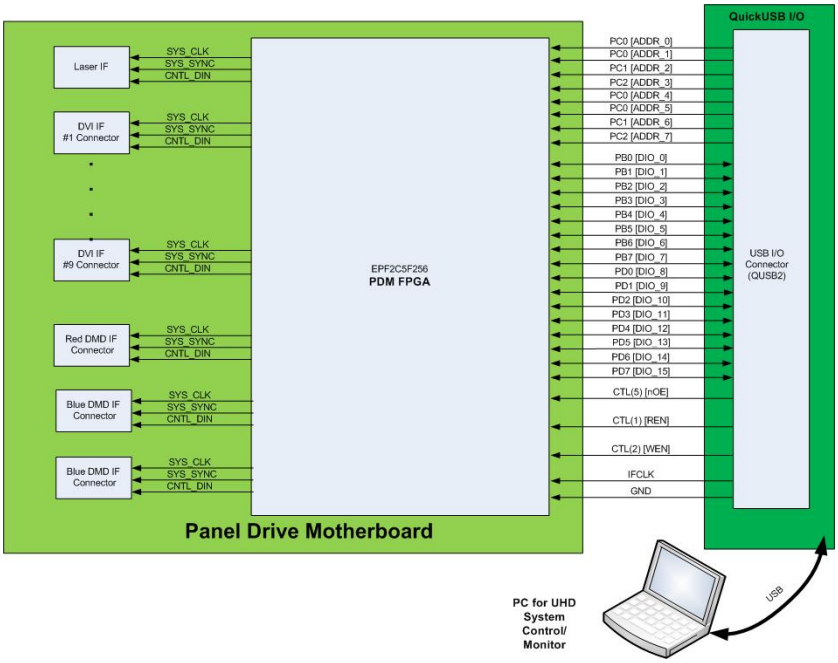


Figure 25 PDM SYS_CLK, SYS_SYNC and CNTL_DIN Distribution

The PDM FPGA creates independent data streams that are synchronized to the SYS_CLK and SYS_SYNC signals and are routed to each module. Each module decodes the serial stream and uses the resulting data as general purpose control bits for configuring test modes, test patterns and setting system parameters. The same SYS_CLK and SYS_SYNC signals are used for video transfer and synchronization.

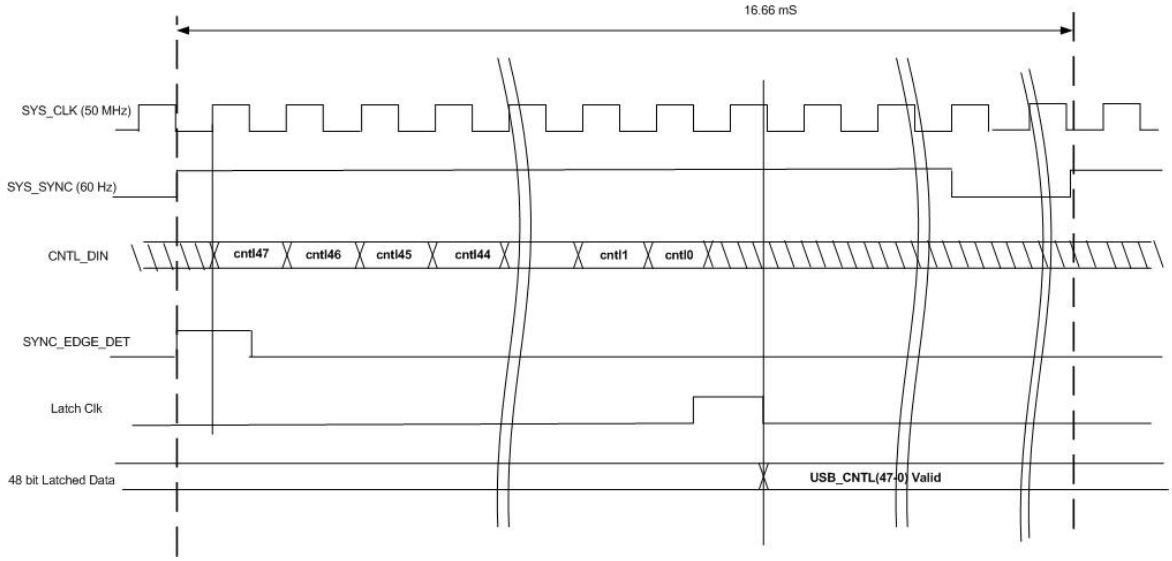


Figure 26 PDM Serial Control Interface Timing

The first 48 bits of each CNTL_DIN stream after the rising edge of the SYS_SYNC signal contains the 48 general purpose control bits for that module. On each module, the CNTL_DIN

serial stream should be routed through a serial to parallel converter and then the parallel data should be latched 48 clocks after the rising edge of SYS_SYNC.

6.1.5. QUSB Interface to Module Serial Interface Memory Map

Each of the 16 bit I/O operations from the QUSB module is accompanied by an 8 bit address. The PDM FPGA decodes these addresses and maps the data to the serial interfaces as follows:

6.1.6. Connection to Laser Interface

A connector is provided on the PDM to supply a differential SYS_CLK, SYS_SYNC, CNTL_DIN and SYS_RST_F to the Laser Interface. Two shielded twisted pair cables should be used to provide the interconnect between the PDM and Laser Interface.

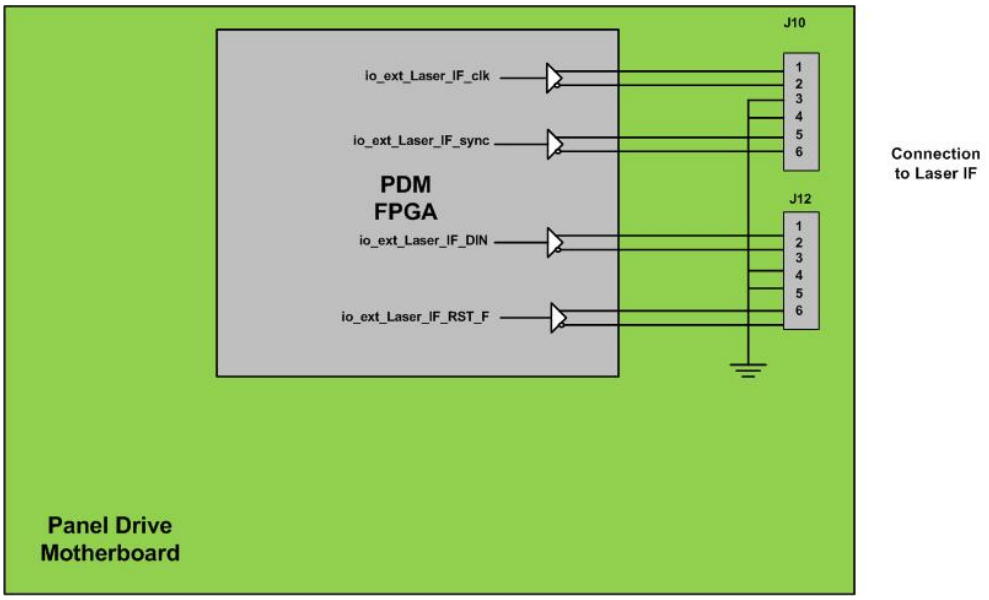


Figure 27 PDM to Laser Interface Connectors

6.2. DMD Interface

The DMD interface is a PCB that interfaces to a TI Discovery 3000 DLP Adapter for driving red, green or blue Digital Micro Mirror Displays (DMD). The DMD interface receives system timing and synchronization from the panel drive motherboard. The 8 bit (red, green or blue) video data from all nine DVI RX IF PCBs is distributed to each DMD Interface via the PDM by16 bit differential pairs. One DMD Interface processes the incoming data through an image buffer that transfers the data to a DMD dedicated for the RED component of the video. Identical DMD interfaces and image buffers transfer the data to DMDs dedicated for the GREEN and BLUE components of the Video. Each DMD Interface receives encoded 8 bit red, green or glue video data as 12 bit gray scale time slice values. These values are stored in 12 different sections of the image buffer, with each section containing a gray scale weight of the complete 1400 × 1050 sub-pixel image for that color. When these 12 gray scale weighted images are written to each DMD in a sequence that is synchronized with a repeating laser intensity pattern, a gray scale level from 0-255 is created for each sub-pixel.

6.2.1. Image Buffer

6.2.1.1. Image Storage

Twelve 1400 × 1050 bit images are stored in an SDRAM image buffer on the DMD Interface for each 1400 × 1050 byte input from each of the nine DVI receiver interfaces.

6.2.1.1.1. Data Input

Each of the three DMD Interface DMD FPGAs receives nine sets of 16 bit differential data busses at the 100 MHz SYS_CLK rate, one from each DVI_RX_IF. Each 16 bit bus consists of two 8 bit video samples for the color dedicated to that FPGA. A total of 1.47 Million (1400 ×1050) bytes are received by each FPGA every 16.66 ms (60 Hz Refresh Rate). The original sequential data bytes from the DVI receiver Interfaces has been re-organized to achieve higher resolution when combined with other DVI_RX_IF outputs prior to being input to the panel drive DMD FPGAs. The input data stream is synchronized to the SYS_SYNC.

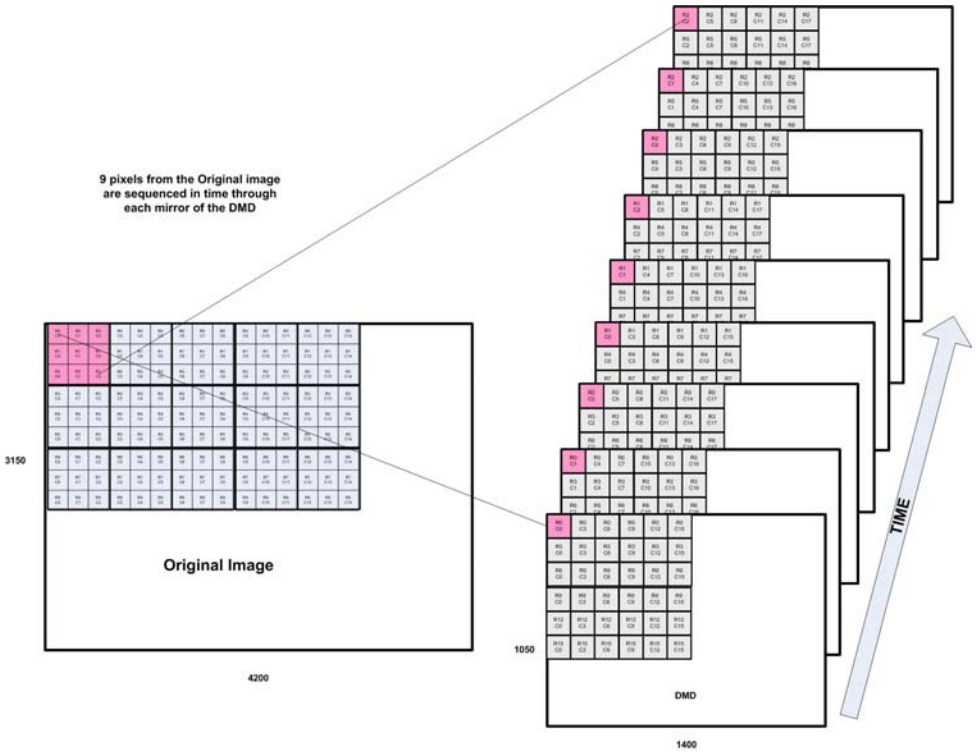


Figure 28 Nine Input Pixels Sequenced in Time for Each DMD Mirror

6.2.1.2. Data Re-organization

From a system standpoint, the order of the RGB data received by each DVI_RX_IF must be re-organized to achieve high resolution and gray scale via a single DMD per color. Ideally, data could be written into the DMD interface image buffer as it is received sequentially from the DVI_RX_IF image buffer and then read out in the order required for expanded resolution and gray scale. Unfortunately, the DDR SDRAMs used for the image buffers transfer data in bursts of sequential addresses and would incur substantial performance hits if individual per byte addressing was used. Therefore, to achieve the SDRAM access performance required on the panel drive motherboard, multiple bytes of data from the DVI_RX_IF image buffer will be latched, re-ordered and transferred in bursts to sequential addresses in SDRAM on the panel drive motherboard.

Since the DMD can only display one ninth of the total resolution for any given frame, the sequence of data being transferred must be re-organized in bursts of multiple bytes from every third pixel. Re-ordering of the sequential data from the DVI_RX_IF before it is transferred to the panel drive mother board accomplishes this.

6.2.1.3. 9X Resolution Transport

Nine 1400 × 1050 DVI inputs to the UHD projector are used to transport a 4200 × 3150 image at a 60 Hz refresh rate. Each of the nine DVI inputs is standard 24 bit color 1400 × 1050 @ 60 Hz sources that could independently be displayed on any standard video monitor capable of SXGA+ resolution.

Each DVI transports one ninth of the original 4200 × 3150 image as a standard 1400 × 1050 image. That is, DVI #1 transports the top left ninth of the original 4200 × 3150 image, DVI #2 transports the top middle ninth, DVI #3 transports the top right, DVI #4 transports the middle left ninth, and so on with DVI #9 transports the bottom right ninth.

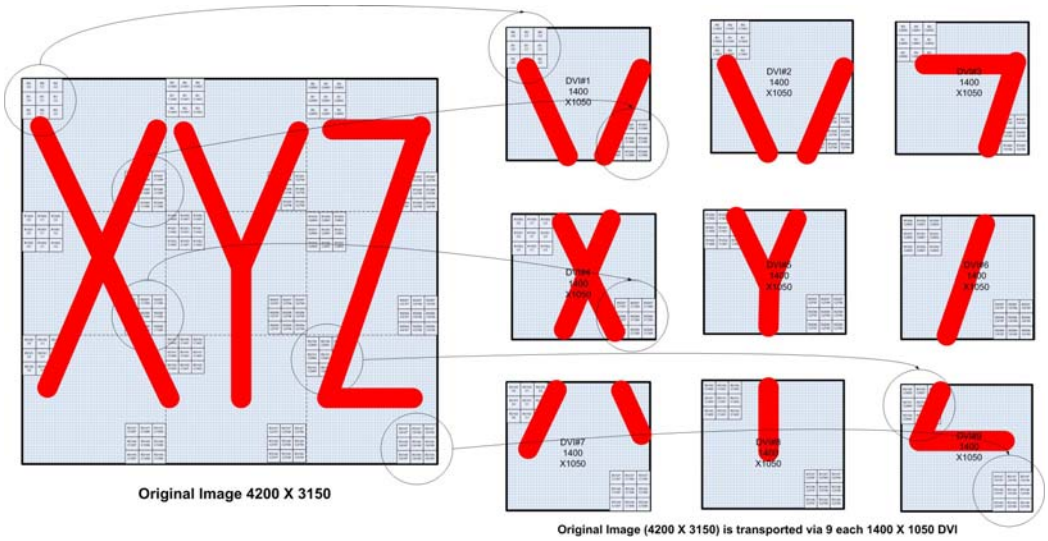


Figure 29 4200 × 3150 Image Transport

6.2.1.4. 9× Resolution on 1400 × 1050 DMD

To achieve high resolution (4200 × 3150) with a 1400 × 1050 DMD the DMD must sequence through nine complete images at nine times the normal rate. Each image is made up from every third pixel per row and every third row of the original 4200 × 3150 image. Each of the nine images is synchronized to illumination focused for that sub-pixel location that when displayed in rapid succession creates a higher resolution image than the DMD is capable of.

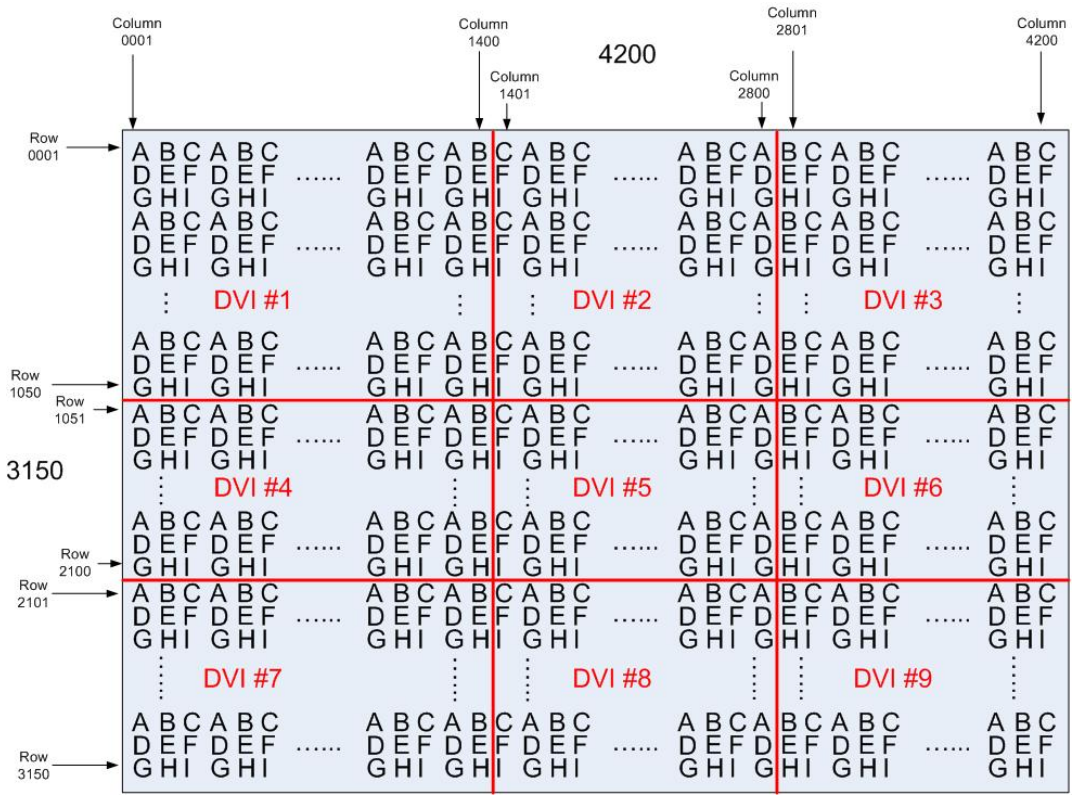


Figure 30 Sub-pixel Type Definition and DVI transport of 4200 × 3150 Image

6.2.1.5. Sub-pixel Partitioning of the High Resolution Image

The pixel in the first row and first column of the 4200 × 3150 image is designated as $A_{R0001/C0001}$ and is an "A" type sub-pixel. The pixel in the first row and second column is designated as $B_{R0001/C0002}$ and is a "B" type sub-pixel. The pixel in the first row and third column is designated as $C_{R0001/C0003}$ and is a "C" type sub-pixel. Starting from the 1st column, every third pixel in the first row (1st, 4th, 7th, ….4198th columns) are "A" sub-pixels. Likewise, starting from the 2nd column, every third pixel in the first row (2nd,5th,8th,….4199th columns) are "B" sub-pixels and starting from the 3rd column, every third pixel in the first row (3rd,6th,9th,….4199th columns) are "C" sub-pixels.

Starting from the 1st column, every third pixel in the second row (1st, 4th, 7th, .4198th columns) are "D" sub-pixels. Likewise, starting from the 2nd column, every third pixel in the 2nd row (2nd,5th,8th,….4199th columns) are "E" sub-pixels and starting from the 3rd column, every third pixel in the second row (3rd,6th,9th,….4200th columns) are "F" sub-pixels.

Starting from the 1st column, every third pixel in the third row (1st, 4th, 7th, .4198th columns) are "G" sub-pixels. Likewise, starting from the 2nd column, every third pixel in the third row (2nd,5th,8th,….4199th columns) are "H" sub-pixels and starting from the 3rd column, every third pixel in the second row (3rd,6th,9th,….4200th columns) are "I" sub-pixels.

This pattern repeats on the forth row with every third pixel in the fourth row (1st, 4th, 7th, ….4198th columns) are "A" sub-pixels. Starting from the second column every third pixel in the fourth row (2nd, 5th, 8th, ….4199th columns)) are "B" sub-pixels, and so on. This pattern continues for all rows, ending with the 3150th row and last 4200th being an "I" sub-pixel.

When data is transferred to the DMD Interface it must be sent in bursts of the same sub-pixel type ("A" thru "I"). Therefore sequential bytes for each color in the incoming data from the DVI receiver will need to be pipelined and then data of the same sub-pixel type will be transferred in bursts to the panel drive motherboard. Starting from the first row, every third row (1st, 4th , 7th , ….3148th rows), needs sub-pixel types "A", "B" and "C" only to be pipelined. Starting from the second row, every third row (2nd, 5th , 8th , ….3149th rows), needs sub-pixel types "D", "E" and "F" only to be pipelined. Starting from the third row, every third row (3rd, 6th , 9th , ….3150th rows), needs sub-pixel types "G", "H" and "I" only to be pipelined. Since rows are received serially only one pipeline register is required. Depending on the current row, the one pipeline register will pipeline sub-pixel types "A", "B", and "C" or sub-pixel types "D", "E" and "F" or sub-pixel types "G", "H" and "I".

6.2.1.6. Re-grouping of Sub-pixel types

To accommodate a DDR burst length of four addresses, 8 bytes of pipeline for each sub-pixel type for each row will be required. A 24 byte pipeline register will capture 8 bytes each for sub-pixel types "A", "B", and "C" , or every third row (1st, 4th , 7th , ….3148th rows), starting from the first row. The same 24 byte pipeline register will capture 8 bytes each for sub-pixel types "D", "E", and "F" , or every third row (2nd, 5th , 8th , ….3149th rows), starting from the second row. Likewise, the same 24 byte pipeline register will capture 8 bytes each for sub-pixel types "G", "H", and "I", or every third row (3rd, 6th , 9th , ….3150th rows), starting from the third row.

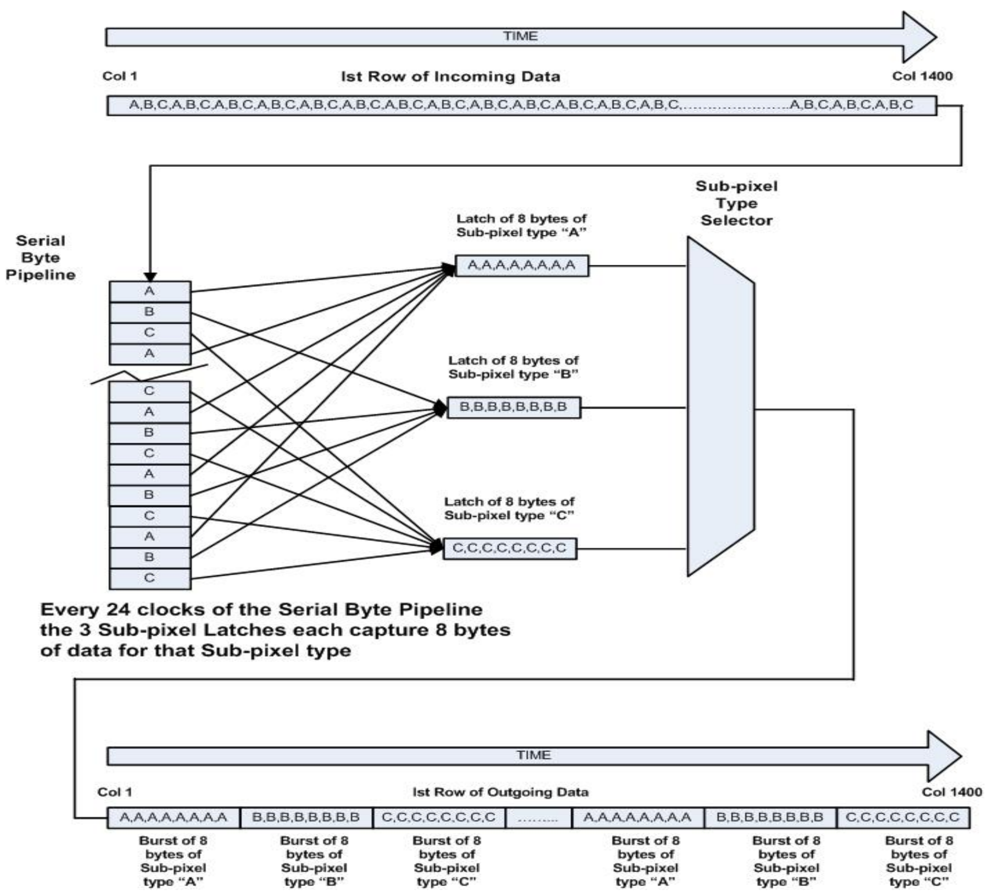


Figure 31 Sub-pixel Type Re-organization

For DVI #1, the diagram above applies to every third row (1st, 4th, 7th, ….1048th DVI rows), starting from the first row. The same diagram applies to sub-pixel types “D”, ”E”, and “F” for every third row (2nd, 5th , 8th , ….1049th DVI rows), starting from the second row. Likewise, the diagram applies to sub-pixel types “G”, ”H”, and “I” for every third row (3rd, 6th, 9th, ….1050th DVI rows), starting from the third row.

6.2.2. FPGA Design

An 1148 pin Virtex-4 FPGA controls the DVI to DMD conversion for the UHD projector. Each Virtex-4 FPGA is dedicated to receiving nine DVI data busses and driving one DMD for a single color (red, green, or blue).

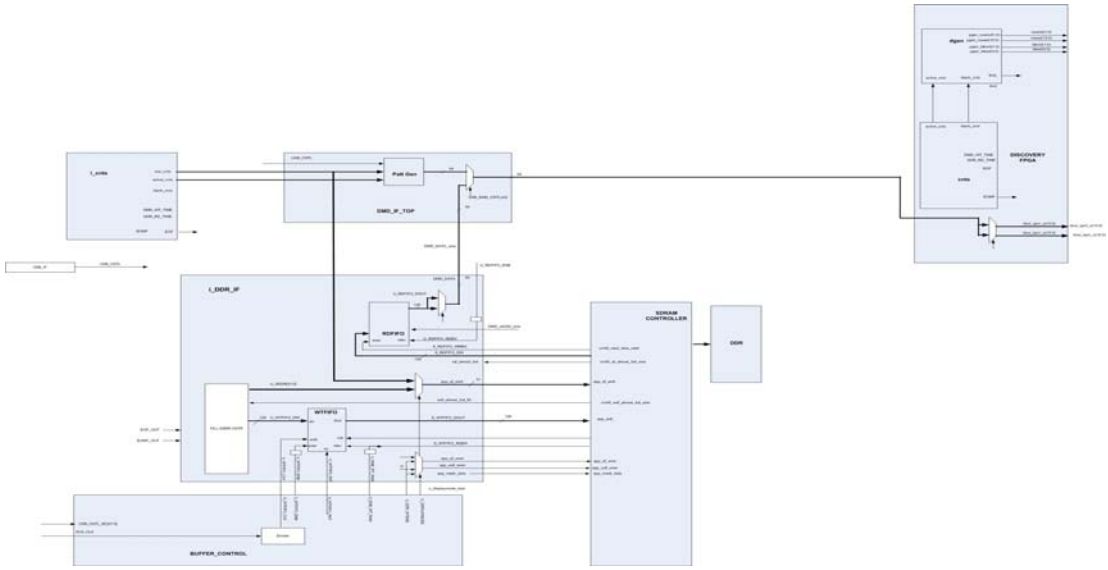


Figure 32 DMD Interface Block Diagram

6.2.3. FPGA I/O Bank Partitioning

Each 1148 pin Virtex-4 FPGA, referred to as the **DMD FPGA**, controls DVI red, green, or blue DVI data collection, storage of the data in SDRAM and transfer of the data to the DMD for each RGB color. The FPGA I/O banks are partitioned to provide various types of electrical interfaces for different interface functions.

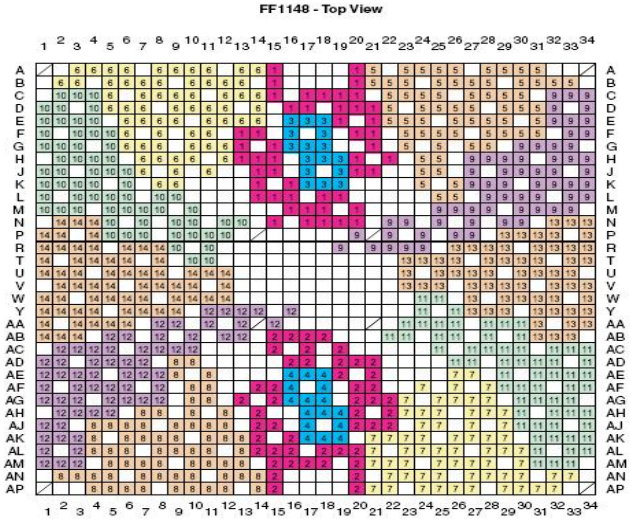


Figure 33 DMD FPGA

Bank – Expansion Connector, Bank 1, 5, 6 – SDRAM, Bank 9, 10 - DMD Connector
Bank – USB I/F, Bank 12, 8, 2,7,11 – DVI Receiver

6.2.4. System Timing FPGA I/O Bank Partitioning

A 1148 pin Virtex-4 FPGA controls DVI RGB data collection, storage of the data in SDRAM and transfer of the data to the DMD for each RGB color. The FPGA I/O is partitioned to provide various types of electrical interfaces for different interfaces.

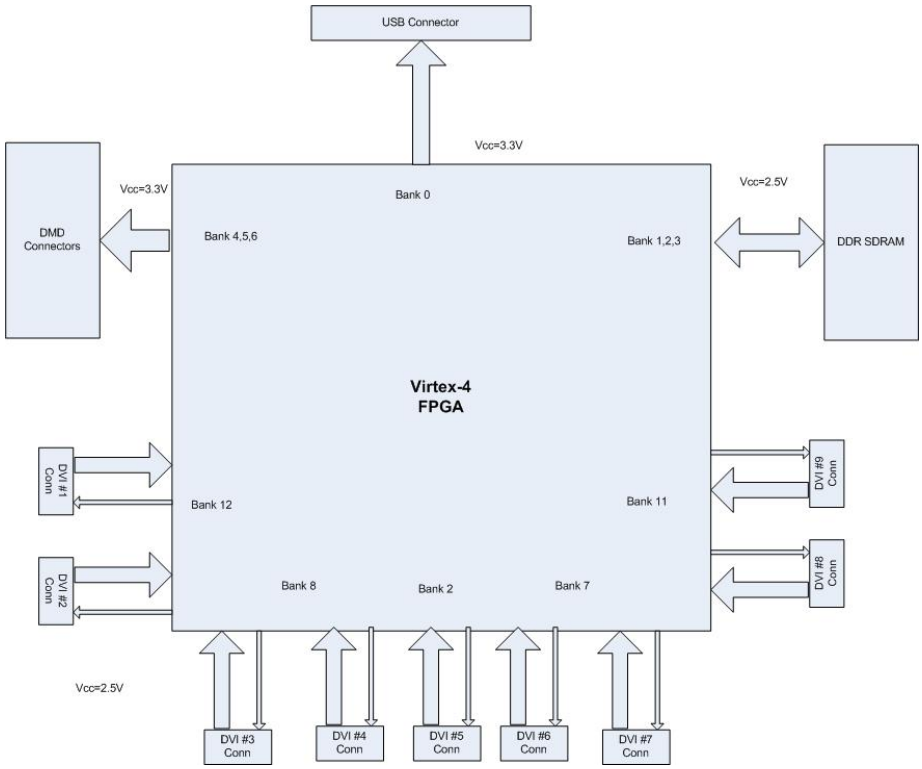


Figure 34 Panel Drive FPGA I/O Banks

- **FPGA I/O Bank 4, 5, 6 – DMD Interface**

Banks 4, 5 and 6 of each of the three DMD Interface DMD FPGAs are configured as 2.5V single ended and differential I/O and are dedicated to transferring the images in the SDRAM image buffer to the DMD for that color.

- **FPGA I/O Bank 12 – DVI Rx Interface #1 and #2**

Bank 12 is configured as 2.5V differential I/O and transports the 16 bit differential bus for that color from DVI Rx Interface #1 and #2.

- **FPGA I/O Bank 8 – DVI Rx Interface #3 and #4**

Bank 8 is configured as 2.5V Differential I/O and transports the 16 bit differential bus for that color from DVI Rx Interface #3 and #4.

- **FPGA I/O Bank 2 – DVI Rx Interface #5**

Bank 2 is configured as 2.5V Differential I/O and transports the 16 bit differential bus for that color from DVI Rx Interface #5

- **FPGA I/O Bank 7 – DVI Rx Interface #6 and #7**

Bank 7 is configured as 2.5V differential I/O and transports the 16 bit differential bus for that color from DVI Rx Interface #6 and #7.

- **FPGA I/O Bank 11 – DVI Rx Interface #8 and #9**

Bank 11 is configured as 2.5V Differential I/O and transports the 16 bit differential bus for that color from DVI Rx Interface #8 and #9.

- **FPGA I/O Bank 1, 2 and 3 – DDR2 Interface**

Banks 1, 2 and 3 is configured as 2.5V single ended and differential I/O and interfaces to a 64 bit × 512MB DDR2 DIMM that stores the images from the DVI receiver interfaces prior to being sent to the DMD for that color.

- **FPGA I/O Bank 0 – USB/GPIO Interface**

Bank 0 is configured as 3.3V CMOS I/O and is connected to a Hirose FX8-80S-SV connector that can be used to interface to a QUICKUSB module for general control and status monitoring of the FPGA during development, or general purpose I/O for logic analyzer and oscilloscope test points.

6.2.5. Image Buffer Pixel Map

To accommodate gray scale, twelve 1400 × 1050 bit images are stored in the DMD image buffer for each 1400 × 1050 byte input from each of the nine DVI receiver interfaces.

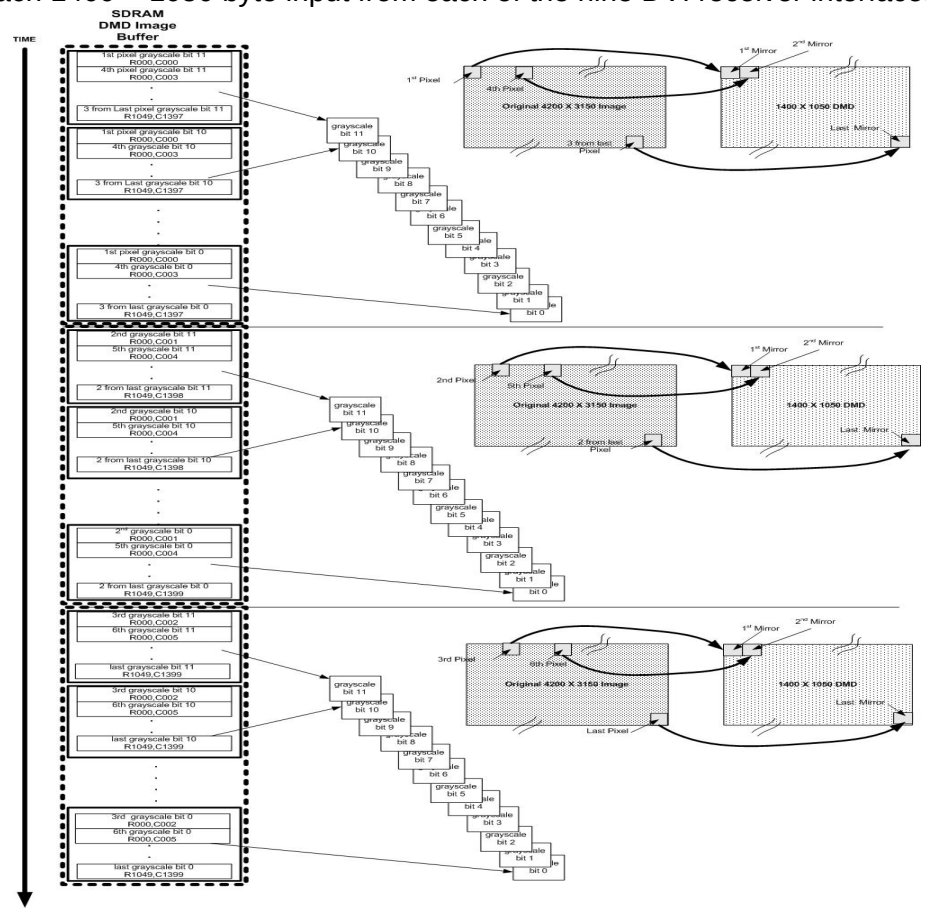


Figure 35 Input Pixel Mapping to DDR2 Image Buffer and DMD

6.2.6. Clock/Sync Generation

The **DMD Interface** receives a differential clock and sync, which it applies to digital clock managers (DCM) in the FPGA. The recovered clock and sync is applied to a VHDL module that is common to the DVI interface FPGA, panel drive motherboard FPGA and the laser interface FPGA.

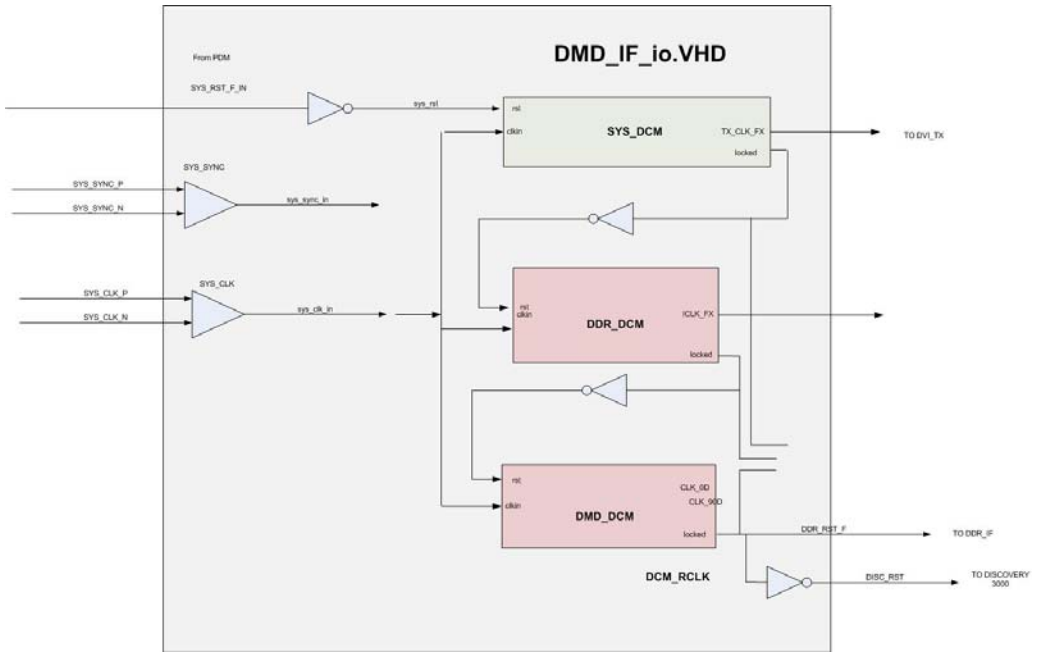
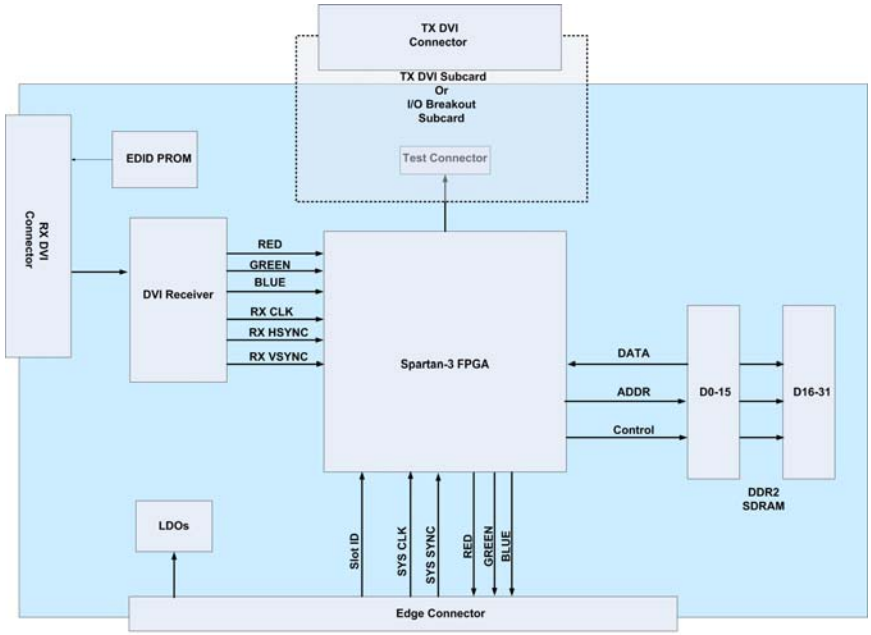


Figure 36 Serial Control Interface

6.3. DVI Interface

The DVI receiver interface (DVI_RX_IF) is a small form factor PCB that interfaces a single standard DVI signal source to the UHD projector. Nine individual 1400 × 1050 DVI_RX_IF cards are used to provide a total resolution input of 4200 × 3150 eight bit RGB pixels @ 60 Hz to the panel drive motherboard. The DVI input is a standard single link LVDS interface with a 118 MHz bit clock (at 60 Hz Refresh Rate).



DVI Rx Interface Block Diagram

Figure 37 DVI Rx Interface Block Diagram

The DVI receiver interface performs the following functions:

- Provides an electrical interface to the serial LVDS DVI inputs and converts signal to digital parallel RGB data and Rx Bit clock and sync
- Buffers complete video frame in SDRAM
  - WRITE FIFO is written at DVI pixel clock rate of 118MHz
  - Write Video Frame is aligned to Rx DVI H/V sync
  - READ FIFO read at 100MHz (1/2 system clock rate)
  - Read Video Frame is aligned to system frame sync
  - Drives red, green and blue video differential 16 bit data pairs to the corresponding DMD
  - Output data order is re-organized for better SDRAM performance on panel drive motherboard
- Supplies EDID display data Information to the PC
- External I/O connector is provided for test purposes

6.3.1. FPGA I/O Bank Partitioning

A 676 pin Spartan-3 FPGA controls DVI RGB data collection, storage of the data in SDRAM and transfer of the data to the panel drive motherboard. The FPGA I/O is partitioned to provide various types of electrical interfaces for different interfaces.

Bank 0 – Expansion connector, Bank 1,2,3 – SDRAM, Bank 4,5,6 – Panel drive motherboard connector, Bank 7 – DVI receiver

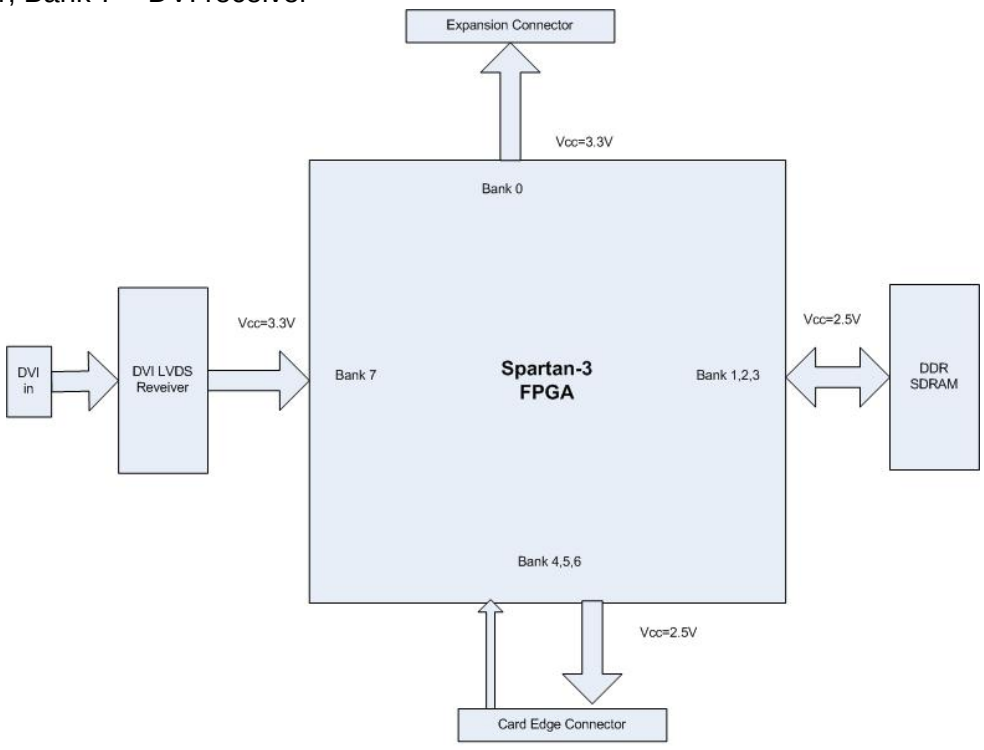
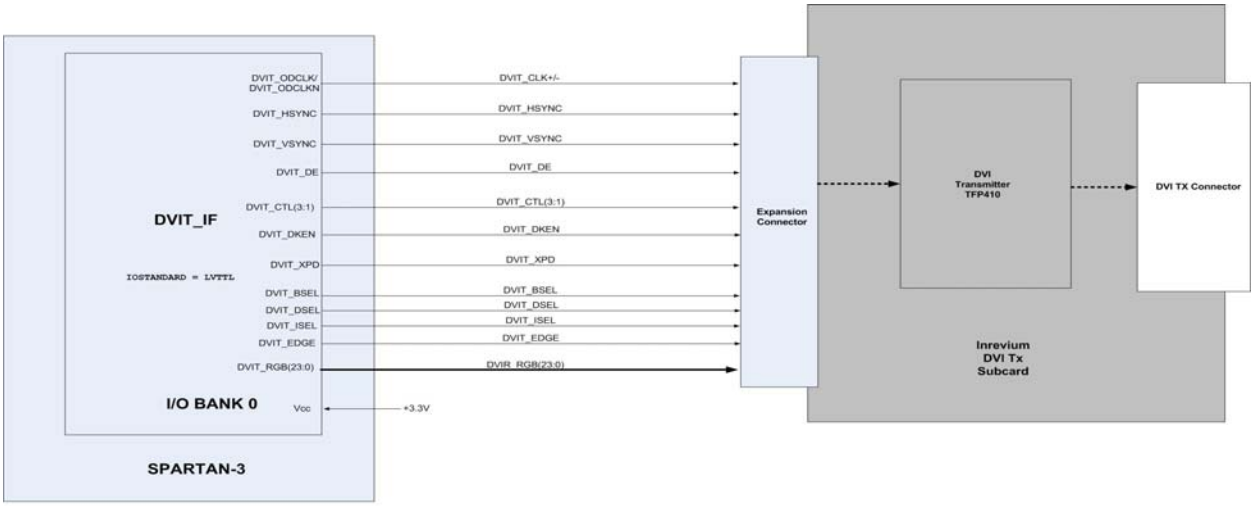


Figure 38 DVI Rx Interface FPGA I/O Banks

6.3.2. FPGA I/O Bank 0 – DVI TX/GPIO

Bank 0 is configured as 3.3V I/O and can be used for test purposes. The signals are routed to an expansion connector that can be connected to an Inrevium sub card. The DVI transmitter

sub card will allow testing of the DVI receiver section of the DVI RX IF by routing the decoded DVI inputs from the receiver to the DVI TX sub card. Alternatively, the Inrevium pin header option sub card can be used for test point access or general purpose I/O (GPIO).

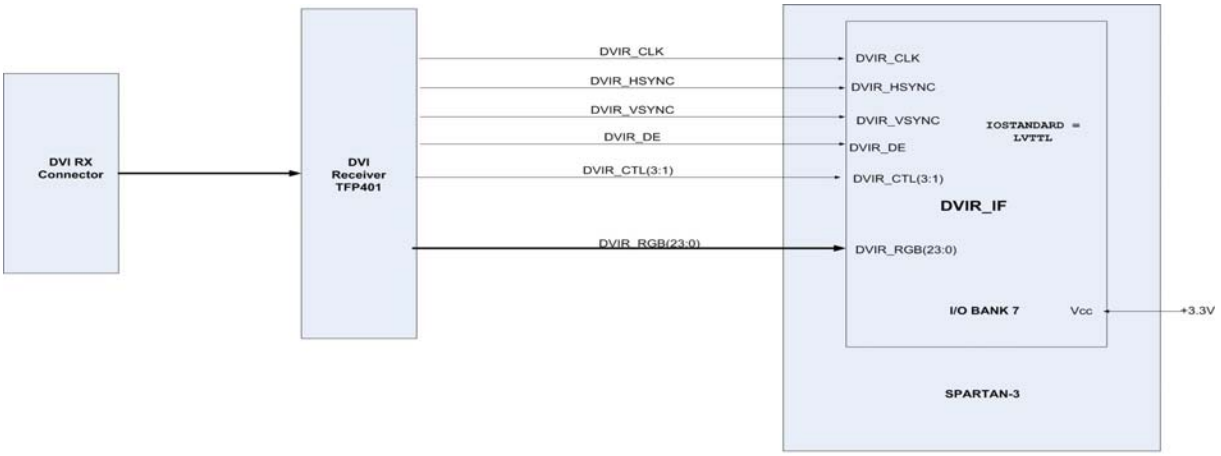


DVI_TX/GPIO Interface

Figure 39 BANK 0 - DVI TX/GPIO Interface

6.3.3. FPGA I/O Bank 7 – DVI RX

Bank 7 is configured as 3.3V I/O and is dedicated to the DVI receiver function. The signals are routed to a TFP401 LVDS serial to parallel interface device.

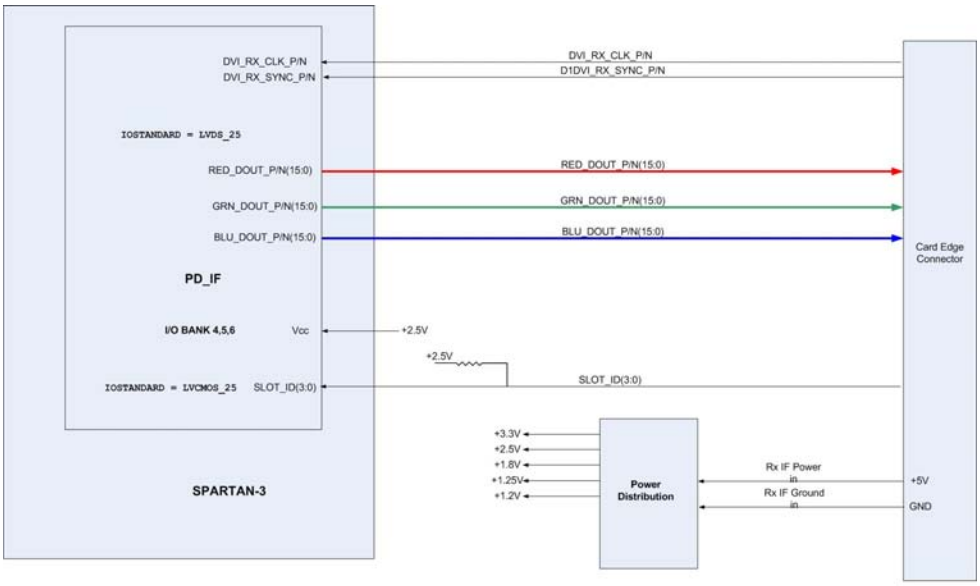


DVI_RX Interface

Figure 40 BANK 7 - DVI Receiver Interface

6.3.4. FPGA I/O Bank 4, 5, 6 – Panel Drive Motherboard

Banks 4, 5 and 6 are configured as 2.5V differential I/O and are dedicated to the panel drive motherboard interface function. The signals are routed to a 164 pin edge connector on the PCB. +5V power for the board and differential system clock and sync signal are input from the edge connector. 16 bit differential red, green, and blue video information is output to the edge connector.

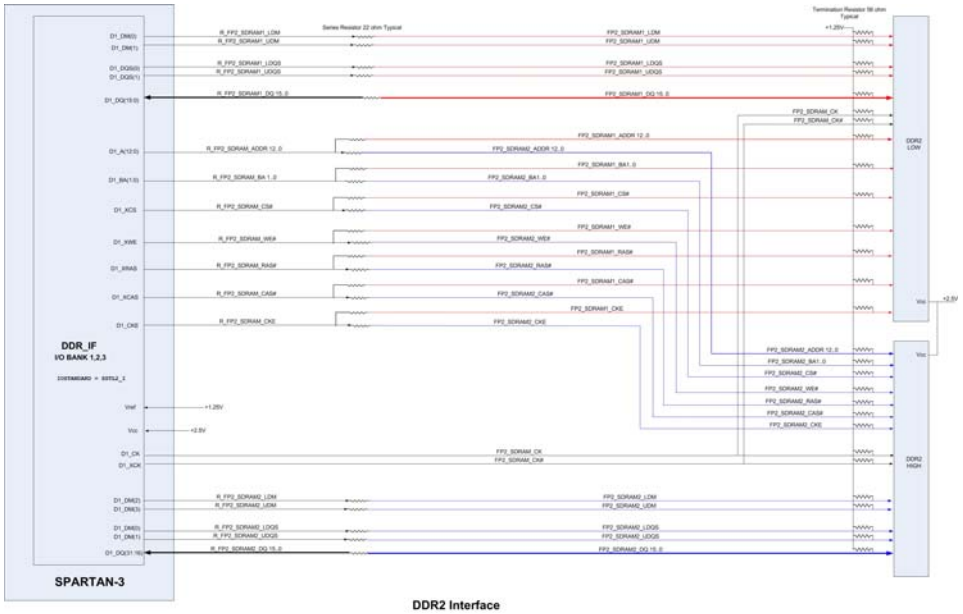


Panel Drive Motherboard Interface

Figure 41 BANK 4, 5, 6 - Panel Drive Motherboard Interface

6.3.5. FPGA I/O Bank 1, 2, 3 – DDR2 Interface

Banks 1, 2 and 3 are configured as 2.5V SSTL_I I/O and are dedicated to the DDR2 interface. Two 512M bit DDR2 SDRAMs (EDD5116AFTA) are used as a video frame buffer. They are configured to create a high speed 32M × 32 bit dual data rate image buffer. An SDRAM Controller in the FPGA manages writing video data that comes in from the DVI interface as well as reading video data from the SDRAM and putting it out on the panel drive motherboard interface.



DDR2 Interface

Figure 42 BANK 1, 2, 3 - DDR2 Interface

6.3.6. FPGA Design

The Spartan-3 FPGA controls timing and orchestrates data flow from the DVI receiver IC to the SDRAM and from the SDRAM to the panel drive motherboard interface. The design is partitioned into several functional modules:

1) CLKGEN
2) DVI_RX
3) (Optional) DVI_TX
4) RGB_TX
5) SRC_SEQ
6) SRAM_DVIT
7) SRAM_DVIR
8) DDR_IF
9) USB_CNTL

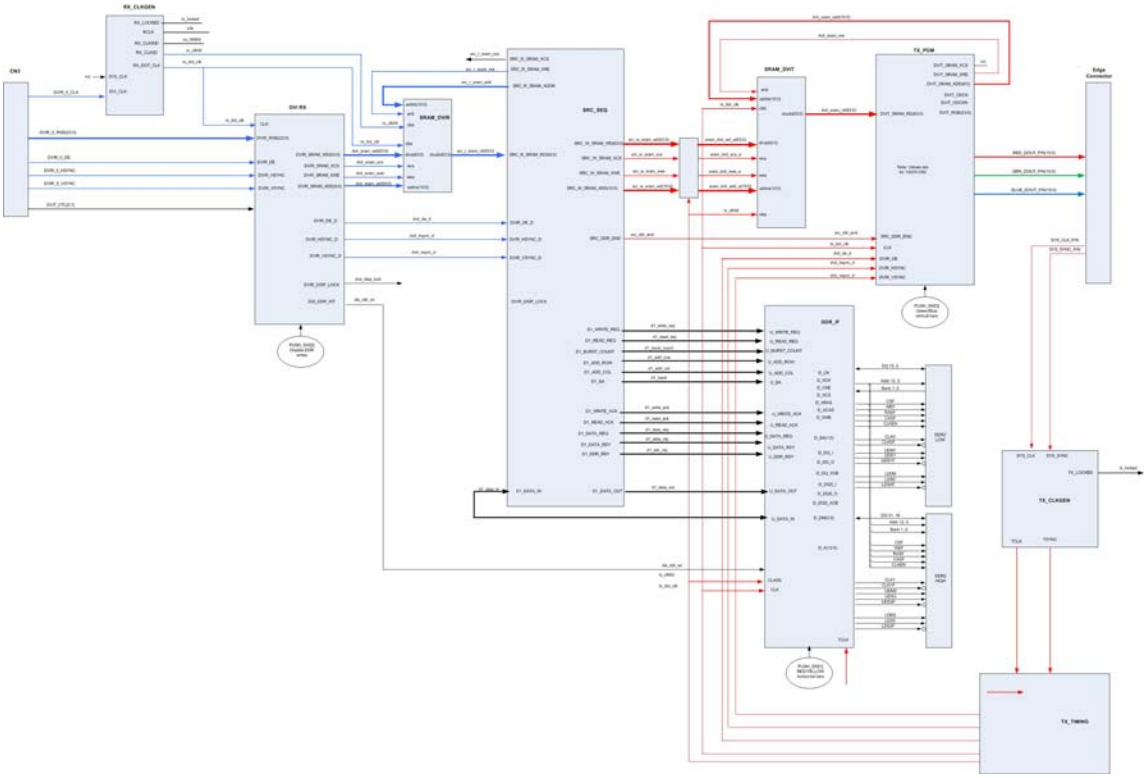


Figure 43 FPGA Block Diagram

- **CLKGEN Module**

The CLKGEN Module contains a DCM that generates a multi-phase clock synchronized to the Rx DVI input clock. The multi-phase clock outputs are used by the DVI_RX module to synchronize, re-time and latch the Receive RGB data inputs from the DVI receiver.

- **DVI_RX Module**

The DVI_RX module latches two sequential instances of the 24 bit RGB data from the DVI receiver creating a 64 bit parallel data bus to be written into the Rx FIFO. 48 of the 64 bits contain RGB data, while 16 bits are set to 0 and are ignored. The DVI_RX module also generates a write address for the Rx FIFO, which increments when the DE signal from the DVI receiver is active.

- **RGB_TX Module**

The RGB_TX module extracts RGB data from the DDR2 image buffer and presents it to the 16 bit RED, 16 bit GRN, and 16 bit BLU differential data busses that the PDM connects to the DMD_IF cards.

Sixty-four bit RGB data from the SRAM_DVIT FIFO is latched by two 24 bit latches which are alternately presented as the 24 bit RGB data to the gray scale module. The SYS_CLK input of

the module sets the rate of the RGB data output to the differential outputs. The SYS_SYNC input synchronizes the transmit RGB frame.

- **Optional DVI_TX Module**

The DVI_TX module can optionally be inserted into the project to test the RGB data integrity from the DVI receiver, through the DDR2 image buffer, to the expansion connector on the PCB. An Inrevium DVI_TX sub-card can be connected to the expansion connector and the RGB path can be verified by connecting a standard SXGA+ DVI capable monitor and viewing that the display properly displays an image presented to the DVI Rx input connector.

Sixty-four bit RGB data from the SRAM_DVIT FIFO is latched by two 24 bit latches which are alternately presented as the 24 bit RGB data to the TL401 DVI transmitter on the Inrevium DVI_TX sub-card. The SYS_CLK input of the module sets the dot rate of the Transmit DVI and all transmit DVI strobe signals (DVIT_VSYNC, DVIT_HSYNC, DVIT_DE) are generated by this clock. The SYS_SYNC input synchronizes the transmit DVI frame.

- **SRAM_DVIR Module**

The SRAM_DVIR module is a 800 × 64 bit FIFO that buffers RGB data from the DVI receiver for writing to the SDRAM. Write control and 64 bit write data come from the DVI_RX Module. Read control comes from the SRC_SEQ module and data read from the FIFO is routed to the SRC_SEQ module prior to going to the SDRAM.

- **SRC_SEQ Module**

The SRC_SEQ module contains a state machine for arbitrating RX and TX FIFO accesses as well as SDRAM accesses. The sequence for accessing SDRAM is as follows:
The Rx FIFO (SRAM_DVIR) begins being filled after the VSYNC input from the DVI receiver.

- **SRAM_DVIT Module**

The SRAM_DVIT Module is an 800 × 64 bit FIFO that buffers RGB data from the SDRAM for writing to the panel drive motherboard Interface. Write control and data come from the SRC_SEQ module. Read control comes from the TX_PDM module and data read from the FIFO is routed to the TX_PDM module.

- **TX_CLKGEN Module**

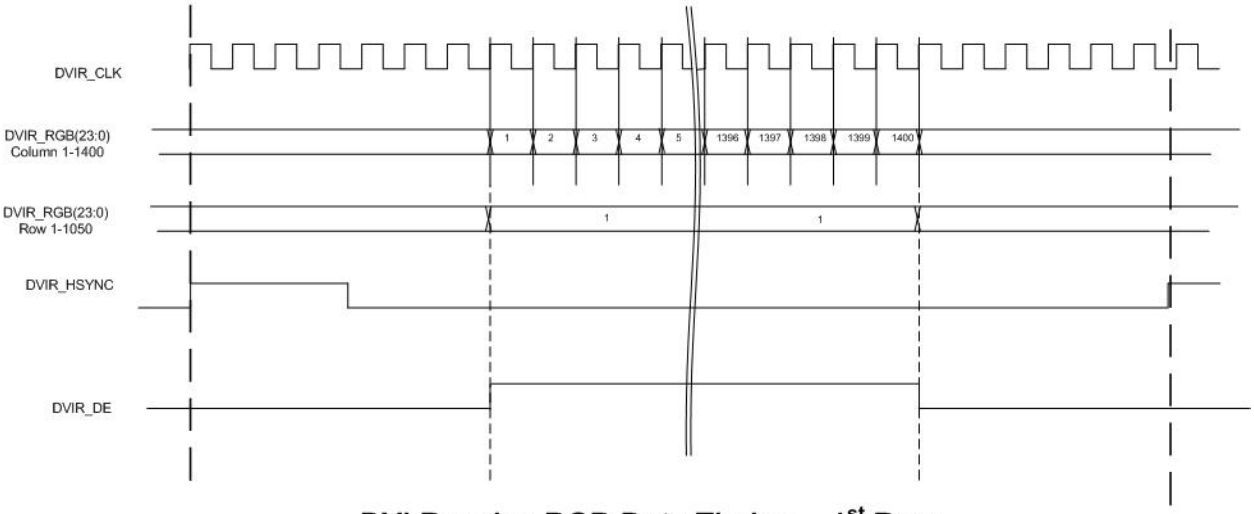
The TX_CLKGEN module contains a DCM that generates a multi-phase clock synchronized to the SYS_CLK input clock. The multi-phase clock outputs are used by the TX_PDM module to synchronize, re-time, and latch the Transmit RGB data outputs going to the panel drive motherboard as red, green and blue 16 bit differential data.

6.3.1. Image Storage

Up to two entire frames of RGB data from DVI receiver are stored in an SDRAM image buffer prior to being sent to the panel drive motherboard.

6.3.1.1. Data Input

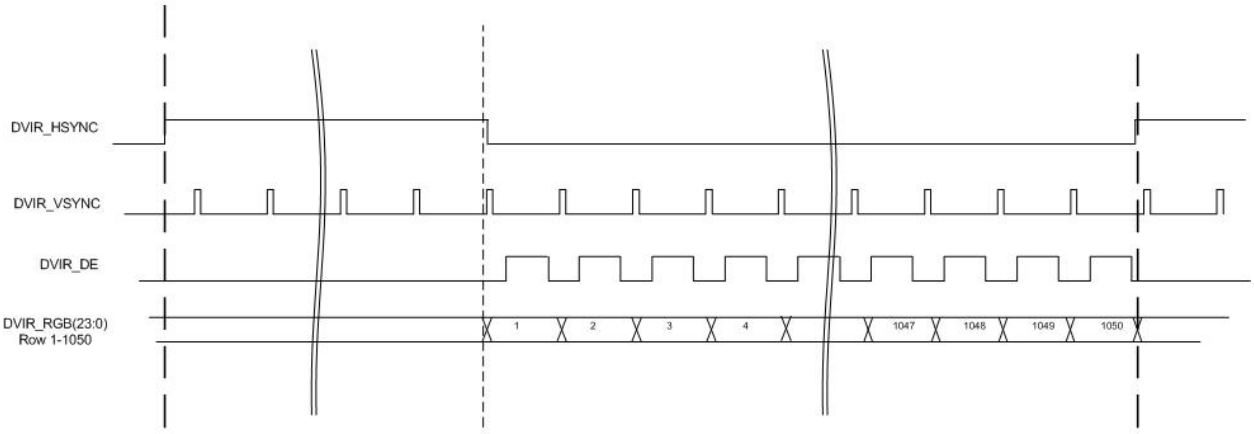
The RGB data is received as 24 bits per 118 MHz clock period, gated by the data enable (DE) signal. The data is received sequentially as 1400 red, 1400 green and 1400 blue bytes per row, synchronized by DVIR_HSYNC.



DVI Receive RGB Data Timing – 1st Row

Figure 44 DVI Rx RGB Data Timing - 1st Row

Each frame, 1050 rows are received sequentially, each row synchronized by DVIR_HSYNC, with a DVIR_VSYNC pulse signifying the end of the frame.



DVI Receive RGB Data Timing – 1050 Rows

Figure 45 DVI Rx RGB Data Timing - 1050 Rows

6.3.2. Data Output

The RGB data read sequentially from the image buffer is transmitted as three individual 16 bit differential data busses at the 100 MHz SYS_CLK rate. Each 16 bit bus consists of two 8 bit video samples for each color. The red, green and blue busses are simultaneously transmitted in parallel with data that has been re-organized to achieve higher resolution when combined with other DVI_RX_IF outputs. The output data stream is synchronized to the SYS_SYNC.

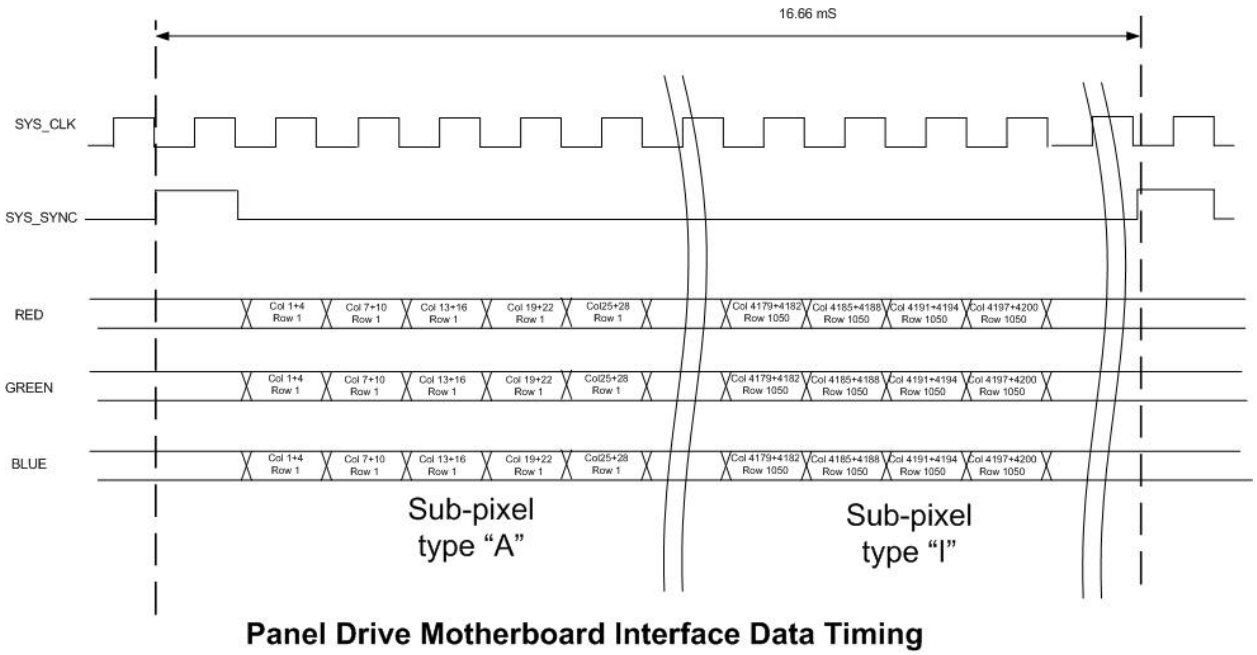


Figure 46 Panel Drive Motherboard Interface Timing

6.3.3. Slot Positions

Because the number of pixels in each row of the DMD is not evenly divisible by 3, the first sub-pixel type to be transferred to the panel drive motherboard is not "A" for all DVIs. DVI #1,#4, and #7 each transport 1050 pixels per row, starting with sub-pixel type "A", followed by repeating "B","C", "A", "B","C", "A","B","C", "A",……, ending with sub-pixel type "B".
DVI #2,#5, and #8 each transport 1050 pixels per row, starting with sub-pixel type "C", followed by repeating "A","B","C", "A","B","C", "A","B","C",……, ending with sub-pixel type "A".
DVI #3,#6, and #9 each transport 1050 pixels per row, starting with sub-pixel type "B", followed by repeating "C","A","B", "C","A","B", "C","A","B",……, ending with sub-pixel type "C".
Each DVI_RX_IF has 4 inputs for slot Identification that can be used to select which sub-pixel pattern to begin and end with. Slot IDs are set by to a unique value for each of the 9 DVI_RX_IF slots.

6.4. Serial Control Interface (Laser Interface)

The **Laser Interface** has a serial control interface for general purpose control of the laser interface. Clock, sync, and data are decoded to create 48 bits that can be used for various test or adjustment controls.

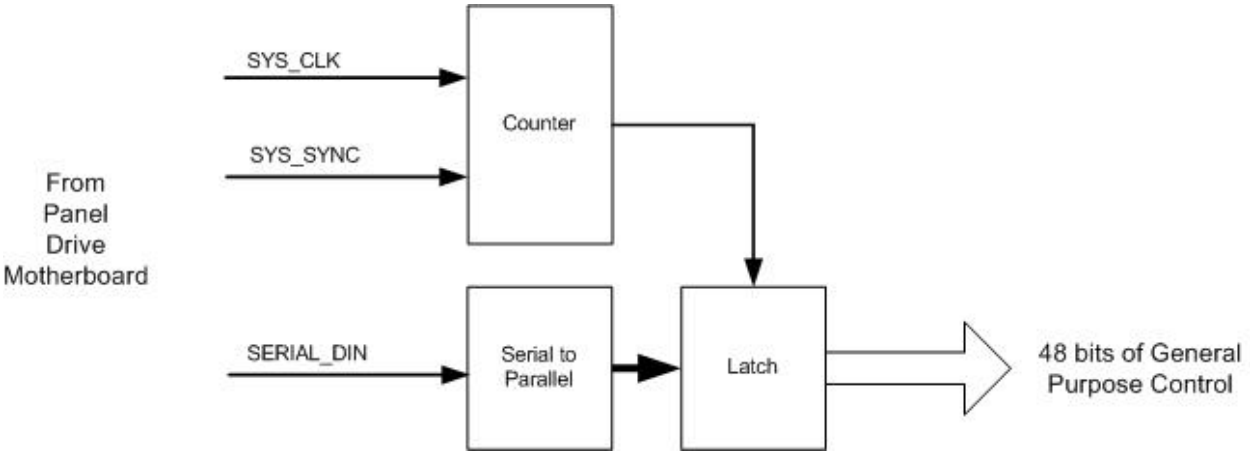


Figure 47 Serial Control Interface

The first 48 bits of each serial_DIN stream after the rising edge of the SYS_SYNC signal contain the 48 general purpose control bits for the laser IF. The serial_DIN serial stream is routed through a serial to parallel converter and then the parallel data is latched 48 clocks after the rising edge of SYS_SYNC.

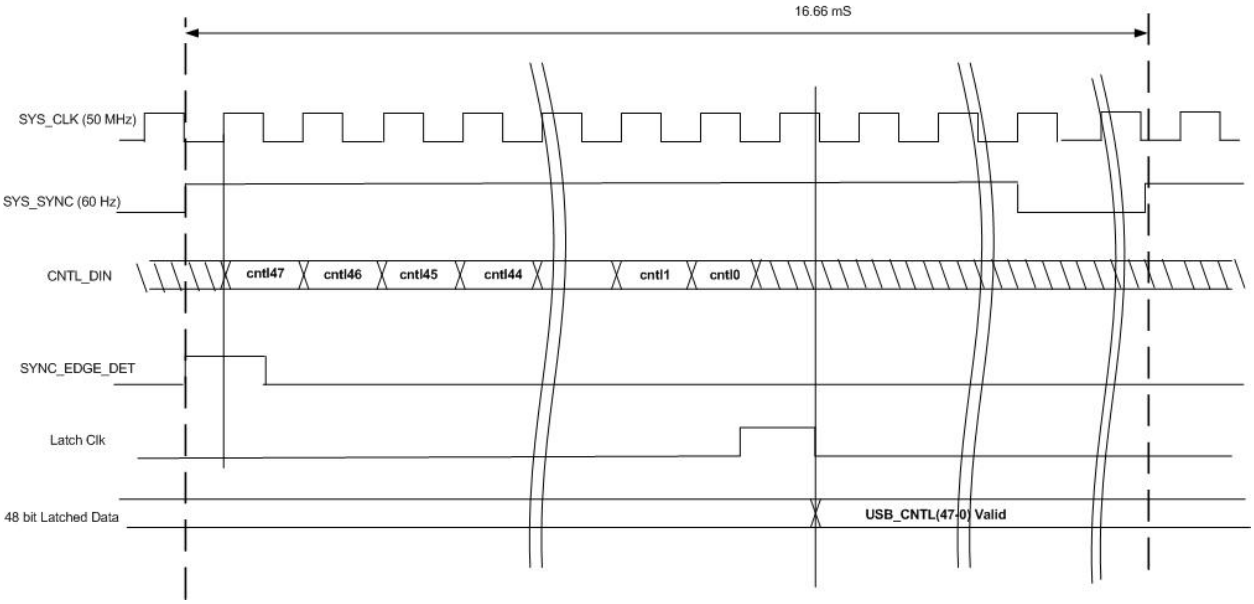


Figure 48 Serial Control Interface Timing

6.4.1. Serial Control Interface Functions

The 48 bit serial control interface allows performance adjustments to the laser IF. It is used to control the DMD interface pattern generator as follows:

Bits 9-0 DMD interface pattern generator control
Bits 25-16 Unused
Bits 41-32 Discovery 3000 control

The DMD interface pattern generator control bits are used for controlling and generating DMD interface based test patterns. The Discovery 3000 control bits are used for controlling

Discovery 3000 configuration bits and controlling and generating Discovery 3000 based test patterns.

6.4.1.1. DMD Interface Pattern Control

The DMD interface pattern generator control bits are defined as follows:
Bit 0 – A '1' enables DMD pattern generation on the video output to the Discovery 3000, while a '0' allows normal operation of buffering video from the DVI interfaces and then transferring it out to the Discovery 3000.

6.4.1.2. Discovery 3000 Control

The Discovery 30000 control bits are defined as follows:
Bit 0 – A '1' enables Discovery 3000 pattern generation on the video output to the DMD, while a '0' allows normal operation sending data from the DMD Interface to the DMD.

Bit 0 – A '1' sets the Discovery 3000 "north/south Flip" bit, while a '0' the clears the Discovery 3000 "north/south Flip" bit.
Bit 0 – A '1' sets the Discovery 3000 "complement data" bit, while a '0' the clears the Discovery 3000 "complement data" bit.

6.5. Deflection System

The deflection system drives an X-axis and Y-axis deflection coil on each of the three laser tubes to steer the electron beam from the electron gun in each tube creating programmable patterns on the crystal in each laser. The deflection system consists of multiple arbitrary waveform generators that are mixed and then amplified to drive the deflection coils. The magnetic field generated by the coils move the position where the electron beam hits the laser crystal at a precise speed in both the horizontal and vertical directions.

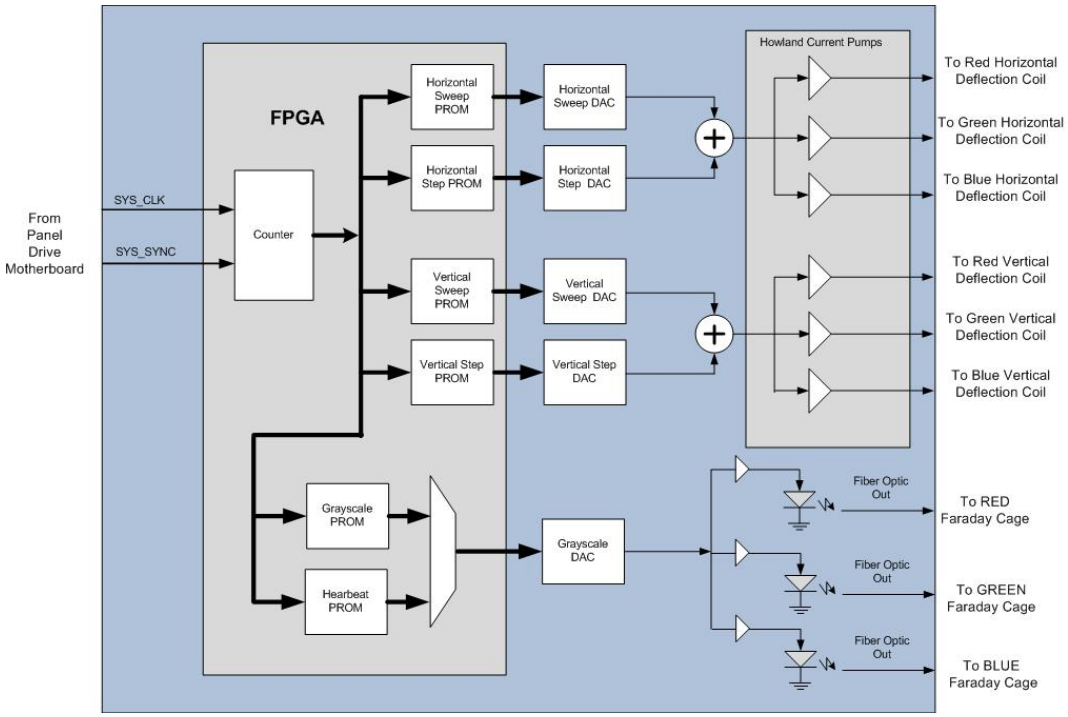


Figure 49 Deflection System Block Diagram

The horizontal sweep arbitrary waveform generator, which is synchronized with the system sync signal, generates a sine wave sweep of decreasing amplitude and decreasing frequency which drives the horizontal deflection coil. Also synchronous with the system sync signal, the vertical sweep arbitrary waveform generator generates a cosine wave sweep of decreasing amplitude and decreasing frequency which drives the vertical deflection coil. The decreasing amplitude on both axes causes the electron beam to move in a circular pattern of decreasing diameter. The decreasing frequency maintains a constant beam speed as the circular pattern diameter decreases.

The circular pattern is periodically moved to one of nine different locations. A horizontal step arbitrary waveform generator that is synchronized to the system sync signal creates three different levels for moving the circular patterns to one of three columns. A vertical step arbitrary waveform generator also synchronized to the system sync signal creates three different levels for moving the circular patterns to one of three rows. The nine different positions are used to create nine sub-pixels for each mirror in the DMD after imaging through the fly's eye lens.

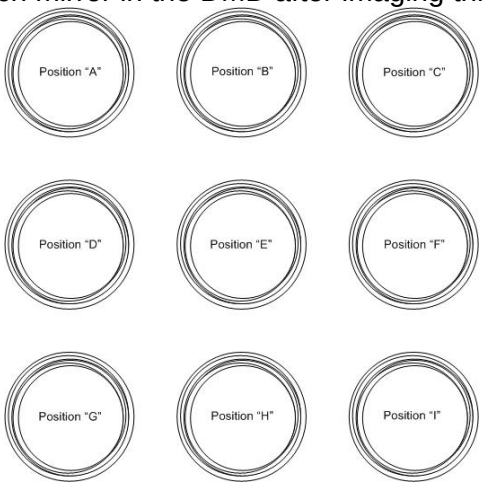


Figure 50 Nine Circular Pattern Positions generated by Deflection System

Additionally, a gray scale arbitrary waveform generator, synchronized with the system sync signal, drives three fiber optic transmitters with a repeating pattern of 12 time slices with six different levels for changing the intensity of the electron beam hitting the crystal in each laser tube. By synchronizing the position of the circular patterns with the gray scale time slices and the position of the 1.47 million mirrors in each of the DMDs for red, blue and green lasers a high resolution projection image with 256 gray scale levels can be created.

The intensity of seven of the 12 gray scale periods are at full scale, one is at ½ full scale, one is at ¼ f full scale, one is at one $1/8^{th}$ full scale, one is at $1/16^{th}$ full scale, and one is at $1/32^{nd}$ full scale. By selecting which of the 12 time slices are reflected by a micro mirror any gray scale level from 0 to 255 can be created for an image. Therefore, each viewable image displayed on the DMD really consists of 12 images in succession that, with the proper time slice selection will appear as one gray scale level image.

A heartbeat pulse is embedded in the gray scale signal transmitted over the fiber optic cable. Each Faraday cage disables the associated laser if this heartbeat is not detected. The heartbeat pulse detector in the Faraday cage is also used to establish the baseline and full scale for the six different gray scale levels.

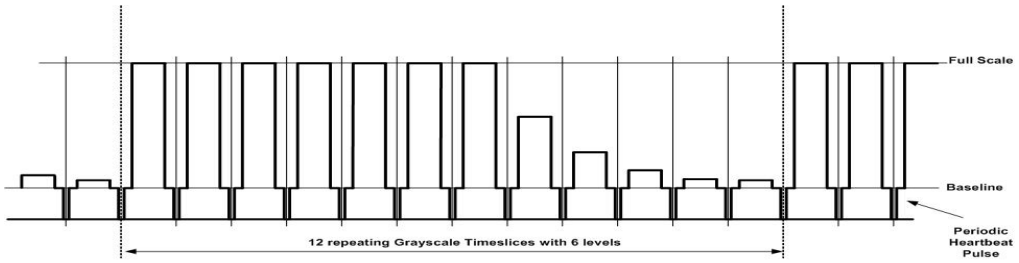


Figure 51 Deflection System Gray Scale Levels

6.6. Laser System Controller

The system controller functional block controls the power up and power down sequence of the laser as well as monitoring the deflection system, system power supplies and system temperatures, and can be used to notify the operator that a problem with the system has been detected and orchestrate a system shutdown.

For the initial “bench model” prototype, the system controller consists of a PC running a custom application that interfaces to a uController in each of the three Faraday cages and three USB data acquisition modules for monitoring and controlling analog and digital inputs and outputs. The PC will allow flexible monitoring and control of the sub-systems of the UHD projector by using commercial off- the-shelf data acquisition and control modules.

The uController in each of the three Faraday cages is interfaced to the PC over full duplex fiber optic serial links. The three USB data acquisition modules each have digital and analog inputs and outputs are conditioned and scaled by three custom analog interface PCBs.

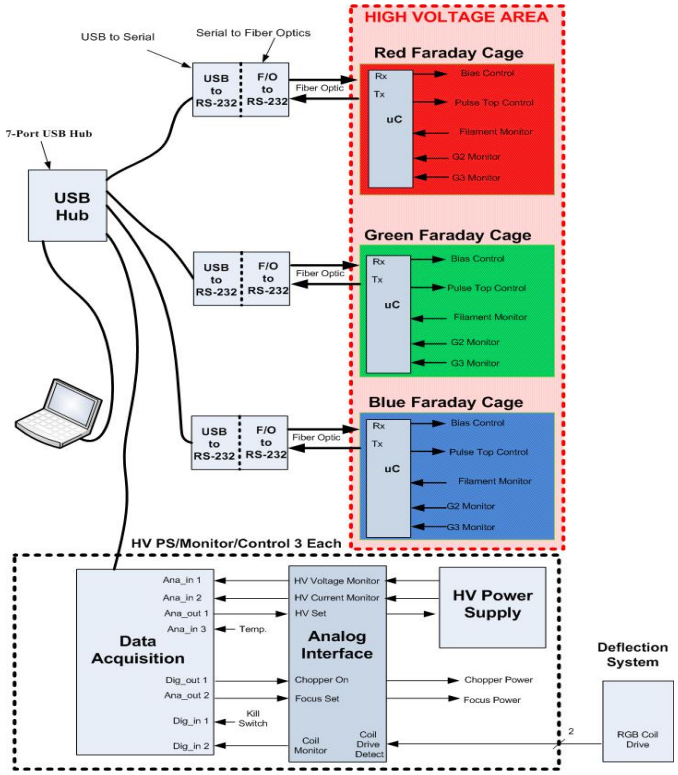


Figure 52 System Controller Block Diagram

6.6.1. System Controller PC Application

A custom software application running on a PC controls and monitors all aspects of the UHD projection system. A Graphical User Interface (GUI) allows visibility of system status and automates the sequence of control of the lasers while monitoring for proper and safe operation. The GUI has menus to allow low level manual control of inputs to the laser electronics as well as top level menus with simple system ON/OFF controls that automatically sequence the individual controls in proper order to orchestrate turning the system on or off. All data from data acquisition monitoring points can be saved in files for post processing. Trends in operating conditions, anomalies and safe operating ranges can be determined by reviewing captured monitor data.

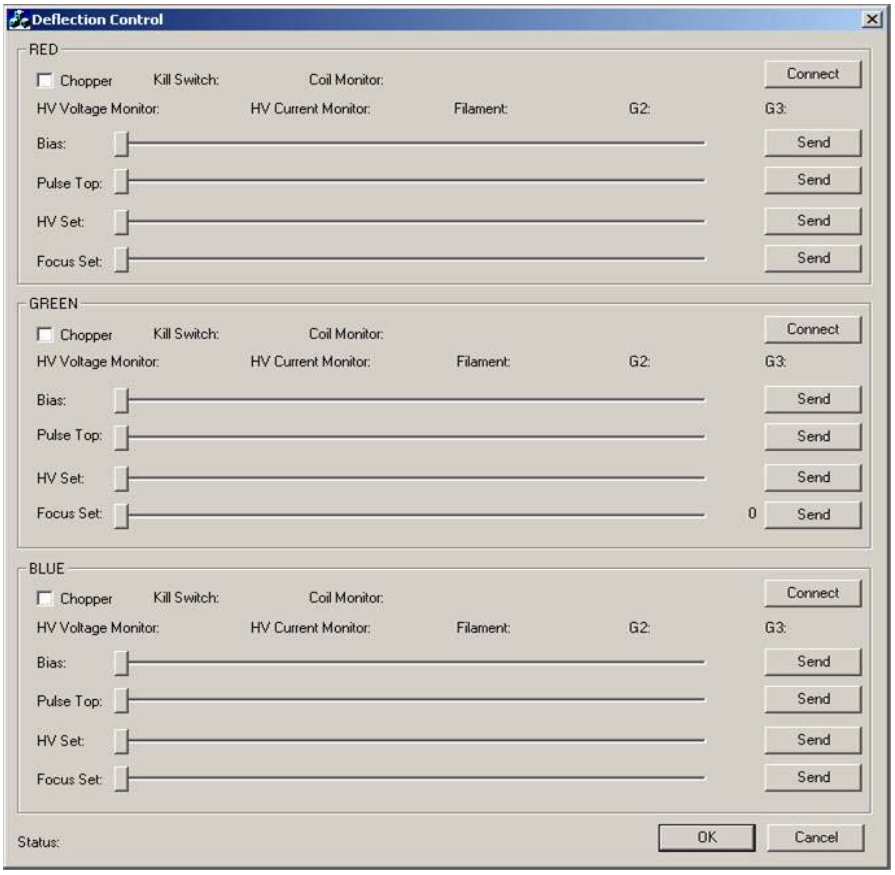


Figure 53 Low Level Menu for controlling the Lasers

6.6.2. Analog/Digital Data Acquisition

The Analog/Digital data acquisition functional block consists of a custom analog interface PCB for signal conditioning and an OTS USB data acquisition modules. Some signals will need level conversion and filtering as well as protection from overvoltage and high voltage arcing before being applied to the USB data acquisition module. The analog interface PCB is connectorized for easy replacement of sensors and flexible placement of the PCB.

Figure 54 Dataq DI-148U USB Data Acquisition Module

6.6.3. Serial Fiber Optic Interface

The serial fiber optic interface functional block consists of off-the-shelf USB to RS-232 adapters and RS-232 to fiber-optic adapters. This will provide multiple standard RS-232 communication links between the PC and the Faraday cages which are biased at -35KV. A microcontroller inside each Faraday cage will be powered from an internal +12V source that is referenced from the -35KV but will be isolated to the rest of the system. The fiber optic link will allow communications between the PC and the microcontroller without any common electrical connection. The serial link between the PC and Faraday cage microcontrollers will be used to set analog and digital controls in the Faraday cage as well as monitor analog and digital status points.

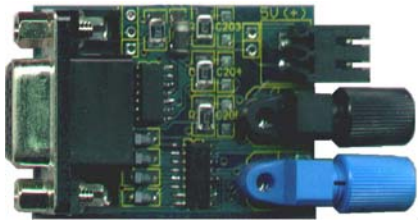


Figure 55 Rigel model RSF Serial to Fiber Optic Adapter

7. PROTOTYPE DEVELOPMENT

7.1. Engineering Design Concept

The Initial SOW for Navy contract N00014-07-C-0664 resulted in the design and fabrication of parts for a full color Light Engine as shown in the diagrams below.

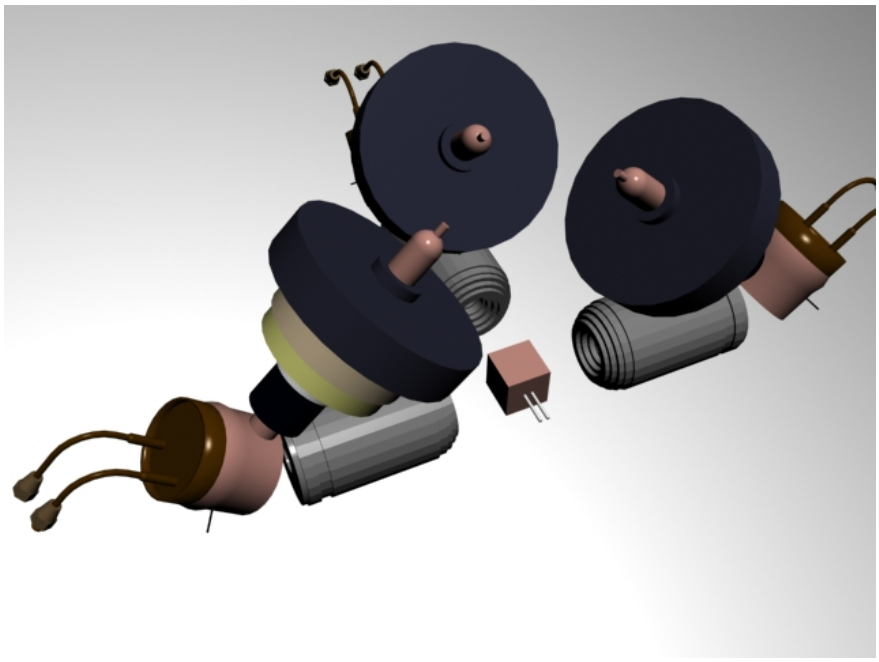


Figure 56 Full Color Laser System

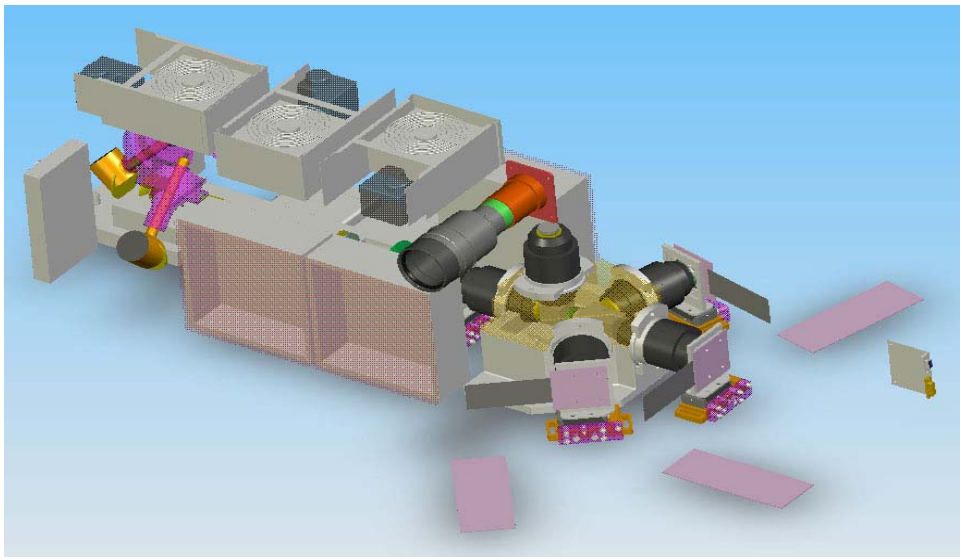


Figure 57 Alpha Model Prototype

After the second contract extension DTI requested additional funding for the completion of the project, however due to government funding shortages this request was not granted. DTI was forced to change the Statement of Work and move forward with a single channel monochrome projector system. DTI obtained a green laser in order to demonstrate the single channel Alpha Prototype. Since at this point the project was out of funds DTI was forced to stop work. At this point in time the UHD projector remains unfinished awaiting additional funds for completion.